IEC 62433-6

Edition 1.0 2020-09

INTERNATIONAL STANDARD

NORME INTERNATIONALE

colour inside

EMC IC modelling –
Part 6: Models of integrated circuits for pulse immunity behavioural simulation – Conducted pulse immunity modelling (ICIM-CPI)

Modèles de circuits intégrés pour la CEM –
Partie 6: Modèles de circuits intégrés pour la simulation du comportement d'immunité aux impulsions – Modélisation de l'immunité aux impulsions conduites (ICIM-CPI)

IEC 62433-6:2020-09(en-fr)

IEC Central Office
3, rue de Varembé
CH-1211 Geneva 20
Switzerland

Tel.: +41 22 919 02 11
info@iec.ch
www.iec.ch

About the IEC
The International Electrotechnical Commission (IEC) is the leading global organization that prepares and publishes International Standards for all electrical, electronic and related technologies.

About IEC publications
The technical content of IEC publications is kept under constant review by the IEC. Please make sure that you have the latest edition, a corrigendum or an amendment might have been published.

IEC publications search - webstore.iec.ch/advsearchform
The advanced search enables to find IEC publications by a variety of criteria (reference number, text, technical committee,…). It also gives information on projects, replaced and withdrawn publications.

IEC Just Published - webstore.iec.ch/justpublished
Stay up to date on all new IEC publications. Just Published details all new publications released. Available online and once a month by email.

IEC Customer Service Centre - webstore.iec.ch/csc
If you wish to give us your feedback on this publication or need further assistance, please contact the Customer Service Centre: sales@iec.ch.

Electropedia - www.electropedia.org
The world's leading online dictionary on electrotechnology, containing more than 22 000 terminological entries in English and French, with equivalent terms in 16 additional languages. Also known as the International Electrotechnical Vocabulary (IEV) online.

IEC Glossary - std.iec.ch/glossary
67 000 electrotechnical terminology entries in English and French extracted from the Terms and Definitions clause of IEC publications issued since 2002. Some entries have been collected from earlier publications of IEC TC 37, 77, 86 and CISPR.

A propos de l'IEC
La Commission Electrotechnique Internationale (IEC) est la première organisation mondiale qui élabore et publie des Normes internationales pour tout ce qui a trait à l'électricité, à l'électronique et aux technologies apparentées.

A propos des publications IEC
Le contenu technique des publications IEC est constamment revu. Veuillez vous assurer que vous possédez l'édition la plus récente, un corrigendum ou amendement peut avoir été publié.

Recherche de publications IEC - webstore.iec.ch/advsearchform
La recherche avancée permet de trouver des publications IEC en utilisant différents critères (numéro de référence, texte, comité d'études,…). Elle donne aussi des informations sur les projets et les publications remplacées ou retirées.

IEC Just Published - webstore.iec.ch/justpublished
Restez informé sur les nouvelles publications IEC. Just Published détaille les nouvelles publications parues. Disponible en ligne et une fois par mois par email.

Service Clients - webstore.iec.ch/csc
Si vous désirez nous donner des commentaires sur cette publication ou si vous avez des questions contactez-nous: sales@iec.ch.

Electropedia - www.electropedia.org
Le premier dictionnaire d'électrotechnologie en ligne au monde, avec plus de 22 000 articles terminologiques en anglais et en français, ainsi que les termes équivalents dans 16 langues additionnelles. Egalement appelé Vocabulaire Electrotechnique International (IEV) en ligne.

Glossaire IEC - std.iec.ch/glossary
67 000 entrées terminologiques électrotechniques, en anglais et en français, extraites des articles Termes et Définitions des publications IEC parues depuis 2002. Plus certaines entrées antérieures extraites des publications des CE 37, 77, 86 et CISPR de l'IEC.

IEC 62433-6

Edition 1.0 2020-09

INTERNATIONAL STANDARD

NORME INTERNATIONALE

colour inside

EMC IC modelling –
Part 6: Models of integrated circuits for pulse immunity behavioural simulation – Conducted pulse immunity modelling (ICIM-CPI)

Modèles de circuits intégrés pour la CEM –
Partie 6: Modèles de circuits intégrés pour la simulation du comportement d'immunité aux impulsions – Modélisation de l'immunité aux impulsions conduites (ICIM-CPI)

INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

COMMISSION
ELECTROTECHNIQUE
INTERNATIONALE

ICS 31.200

ISBN 978-2-8322-8813-9

Warning! Make sure that you obtained this publication from an authorized distributor.
Attention! Veuillez vous assurer que vous avez obtenu cette publication via un distributeur agréé.

CONTENTS

INTERNATIONAL ELECTROTECHNICAL COMMISSION

EMC IC MODELLING –

Part 6: Models of integrated circuits for pulse immunity behavioural simulation – Conducted pulse immunity modelling (ICIM-CPI)

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.

2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.

3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.

4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.

5) IEC itself does not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC is not responsible for any services carried out by independent certification bodies.

6) All users should ensure that they have the latest edition of this publication.

7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.

8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.

9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 62433-6 has been prepared by subcommittee 47A: Integrated circuits, of IEC technical committee 47: Semiconductor devices.

The text of this International Standard is based on the following documents:

CDV	Report on voting
47A/1090/CDV	47A/1098/RVC

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 62433 series, published under the general title *EMC IC modelling*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

IMPORTANT – The 'colour inside' logo on the cover page of this publication indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.

EMC IC MODELLING –

Part 6: Models of integrated circuits for pulse immunity behavioural simulation – Conducted pulse immunity modelling (ICIM-CPI)

1 Scope

The objective of this part of IEC 62433 is to describe the extraction flow for deriving an immunity macro-model of an Integrated Circuit (IC) against conducted Electrostatic Discharge (ESD) according to IEC 61000-4-2 and Electrical Fast Transients (EFT) according to IEC 61000-4-4.

The model addresses physical damages due to overvoltage, thermal damage and other failure modes. Functional failures can also be addressed.

This model allows the immunity simulation of the IC in an application. This model is commonly called "Integrated Circuit Immunity Model Conducted Pulse Immunity", ICIM-CPI.

The described approach is suitable for modelling analogue, digital and mixed-signal ICs. Several terminals of an IC can be part of a single model (e.g. input, output and supply pins). The implementation of the model is capable of representing the non-linear behaviour of overvoltage protection circuits.

The model can be implemented for the use in different software tools for circuit simulation in time-domain. The described modelling approach allows simulating device failure due to ESD or EFT at component and system level considering all components necessary for the immunity simulation of an IC, such as a PCB or external protection elements.

This document demonstrates, in detail, the construction of models in a defined XML-based format which is suitable for the exchange of models without any deeper knowledge of the semiconductor circuit. However, the model functionality can be implemented in different formats including, but not limited to, tables, SPICE[1] [1] netlists, hardware description languages such as VHDL-AMS [2] and Verilog-AMS [3].

This document provides:

- the description of ICIM-CPI macro-model elements representing electrical, thermal or logical behaviour of the IC.
- a universal data exchange format based on XML.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61000-4-2, *Electromagnetic compatibility (EMC) – Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test*

---

[1] Numbers in square brackets refer to the bibliography.

IEC 61000-4-4, *Electromagnetic compatibility (EMC) – Part 4-4: Testing and measurement techniques – Electrical fast transient/burst immunity test*

IEC 62215-3, *Integrated circuits – Measurement of impulse immunity – Part 3: Non-synchronous transient injection method*

IEC 62433-1, *EMC IC modelling – Part 1: General modelling framework*

IEC 62433-4:2016, *EMC IC modelling – Part 4: Models of integrated circuits for RF immunity behavioural simulation – Conducted immunity modelling (ICIM-CI)*

IEC 62615, *Electrostatic discharge sensitivity testing – Transmission line pulse (TLP) – Component level*

3 Terms, definitions, abbreviated terms and conventions

3.1 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- ISO Online browsing platform: available at http://www.iso.org/obp
- IEC Electropedia: available at http://www.electropedia.org/

3.1.1
pulse
abrupt variation of short duration of a physical quantity followed by a rapid return to the initial value

Note 1 to entry: In this document, a pulse can be represented by a voltage or current quantity.

[SOURCE: IEC 60050-161:1990, 161-02-02, modified – Note 1 has been added.]

3.1.2
non-linear
qualifies a circuit (element) for which not all relations between the integral quantities are linear

[SOURCE: IEC 60050-131:2002, 131-11-19]

3.1.3
network
set of ideal circuit elements and their interconnections, considered as a whole

[SOURCE: IEC 60050-131:2002, 131-13-03, modified – The words "in network topology" have been removed at the beginning of the definition as well as the note.]

3.1.4
branch
subset of a network, considered as a two-terminal circuit, consisting of a circuit element or a combination of circuit elements

[SOURCE: IEC 60050-131:2002, 131-13-06]

3.1.5
node
end-point of a branch connected or not to one or more other branches

[SOURCE: IEC 60050:2002, 131-13-07, modified – The US term "vertex" has been removed.]

3.1.6
external terminal
terminal of an integrated circuit macro-model which interfaces the model to the external environment of the integrated circuit

EXAMPLE Power supply pins and input/output pins.

[SOURCE: IEC 62433-2:2017, 3.1.1, modified – The note has been removed.]

3.1.7
internal terminal
terminal of an integrated circuit macro-model's component which interfaces the component to other components of the integrated circuit macro-model

[SOURCE: IEC 62433-2:2017, 3.1.2, modified – The note has been removed.]

3.1.8
performance degradation
undesired deviation in the operational performance of any device, equipment or system from its intended performance

Note 1 to entry: The term "degradation" can apply to both recoverable failure and permanent silicon damage.

3.1.9
hard failure
irreversible failure due to damage of the IC

3.1.10
soft failure
temporary functional failure, self or user recoverable

3.1.11
PPN
Pulse Propagation Network
electrical network that models the propagation network of the disturbance

3.1.12
PDN
Passive Distribution Network
the part of the PPN that represents the linear characteristics of propagation path of electromagnetic noises such as power distribution network

[SOURCE: IEC 62433-2:2017, 3.1.10, modified – The definition has been adapted to linear part of the PPN.]

3.1.13
DI
Disturbance Input
input terminal for the injection of transient disturbances

Note 1 to entry: It could be any pin of IC, an input, supply or an output.

[SOURCE: IEC 62433-4:2016, 3.1.9, modified – The definition has been adapted to transient disturbances.]

3.1.14
DO
Disturbance Output
terminal whose load influences the impedance of DI terminal, and/or the transfer characteristics of PPN, and that outputs a part of the disturbance received on the DI terminals

[SOURCE: IEC 62433-4:2016, 3.1.10, modified – The definition has been adapted to PPN.]

3.1.15
OO
Observable Output
output terminal or internal terminal where the failure criteria are monitored or computed during the test

[SOURCE: IEC 62433-4:2016, 3.1.11, modified – The definition has been adapted to failure criteria.]

3.1.16
NLB
Nonlinear Block
part of the PPN that represents the non-linear characteristics of propagation path of electromagnetic noises such as power distribution network

EXAMPLE: ESD diodes, clamping diodes, back-to-back diodes, active MOS-based protection, silicon-controlled rectifier (SCR)–based protection

3.1.17
FB
Failure Behavioural
block that describes the internal failure behaviour of the IC

3.1.18
VNA
Vector Network Analyser
network analyser capable of measuring complex values of the S-parameters

[SOURCE: CISPR 16-1-4:2019 3.1.21, modified – The definition has been adapted so as not to limit to 4-port VNA]

3.1.19
CPIML
Conducted Pulse Immunity Markup Language
data exchange format for ICIM-CPI macro-model

3.1.20
CPIMLBase
Conducted Pulse Immunity Markup Language Base
abstract type from which all CPIML model components are directly or indirectly derived in the ICIM-CPI model definition

3.1.21
parser
tool for syntactic analysis of data that is encoded in a specified format

3.1.22
section
XML element placed one level below the root element or within another section and that only contains one or more child elements (no character data, for example)

3.1.23
parent
keyword which is one level above another keyword (child)

3.1.24
child
keyword which is one level below another keyword (parent)

3.2 Abbreviated terms

EFT	Electrical Fast Transient
ESD	ElectroStatic Discharge
SPICE	Simulation Program with Integrated Circuit Emphasis
TLP	Transmission Line Pulse
VHDL-AMS	Very high speed integrated circuits Hardware Description Language – Analog and Mixed Signal
XML	eXtensible Markup Language

3.3 Conventions

For the sake of clarity, but with some exceptions, the writing conventions of XML language have been used in text and tables.

The symbol "µ" is used in the text part to define micro = 1e-6. The symbol "u" is used in the XML parts to define micro = 1e-6.

4 Philosophy

With shrinking transistors and lowering operating voltages, the IC manufacturers and users have especially to take care on the immunity of their products to fast transient electrical stresses such as ESD and EFT. An ESD may be caused by component handling or assembly. An EFT may be caused by a switching event. The amplitude of these stresses ranges from hundreds of Volts to several tens of kV and/or from a few Amperes to tens of Amperes, their duration from tens to hundreds of nanoseconds.

To prevent failure of electronic products due to transient stresses, various tests have been designed. The IEC 61000-4-2 and IEC 61000-4-4 are used to evaluate system components robustness to ESD and EFT respectively.

The TLP test described in IEC 62615 is often used to characterise non-linear device I/V curves of on-chip and off-chip protection circuits. However there are different ways to extract and implement behavioural models for system level ESD and EFT simulation in descriptive languages such as SPICE, VHDL-AMS, and Verilog-AMS. Models which are suitable to cover the ESD and EFT domain allow system designers to simulate protection performance. The purpose of the simulation using these models is to reduce the number of prototyping cycles, reduce time and cost. To be readily available, these models are recommended to be expressed in a standardized exchange format.

The proposed model describes the electrical characteristics of the pulse propagation path and the functional behaviour of the IC affected by that transient event. The electrical network, the Pulse Propagation Network (PPN), propagates the transient pulse into the IC. This network represents linear effects via the Passive Distribution Network (PDN) and the non-linear effects

via the Non-linear Block (NLB), respectively. The voltage, current and energy affecting the IC can be calculated in a circuit simulator (e.g. SPICE) by modelling the PPN. These voltage, current and/or energy may cause failure, as described by the Failure Behavioural (FB) block of the model. Comparing the simulated voltage, current and energy with the thresholds contained in the FB, failure can be predicted. Multiple failure mechanisms (e.g. overvoltage and overheating) can be described by the FB. Moreover, various classes of performance can be predicted (i.e. hard and soft failures). Clause 5 defines the model structure in detail.

To allow easy exchange of models, the ICIM-CPI model data is arranged in a human and machine-readable, nested manner using the XML format. Clause 6 defines how the model structure maps to the XML format called Conducted Pulse Immunity Mark-up Language (CPIML).

5 ICIM-CPI model structure

5.1 General

The internal structure of an IC can be broken down into two parts:

- Passive part: parasitic elements of pins, bonding and tracks, etc., which conduct the disturbances from the external environment to the internal IC blocks,
- Active part: CPU core, clock system, memory, analogue blocks, ESD protection, etc., which are sensitive to the incoming pulse disturbances.

An ICIM-CPI model is used to predict the pulse immunity level of an IC as illustrated in Figure 1. The ICIM-CPI model consists of a set of data describing three parts:

- PDN: the passive distribution network that describes the linear characteristics of the devices in the pulse propagation path
- NLB: the non-linear block that describes the non-linear characteristics of the devices in the pulse propagation path
- FB: the failure behavioural component that describes the failure behaviour of IC regarding to the applied disturbances. FB contains also the failure criteria and the time domain waveform if needed.

The PDN and NLB together form the pulse propagation network (PPN).

The disturbance is applied to the external terminal T1 which is considered as the DI (Disturbance Input). The disturbance can flow out of the IC through the terminal T2 which is considered as the DO (Disturbance Output). The effect of the disturbance is observed at the OO (Output Observable). The signal at OO could be monitored or computed on external terminal (for example OO1 is measured on T3 in Figure 1) or monitored or computed on internal terminal (for example OO2 is computed on IT1 in Figure 1). According to the failure criteria defined in the FB and applied to the OO, the failure level caused by the disturbance could be evaluated.

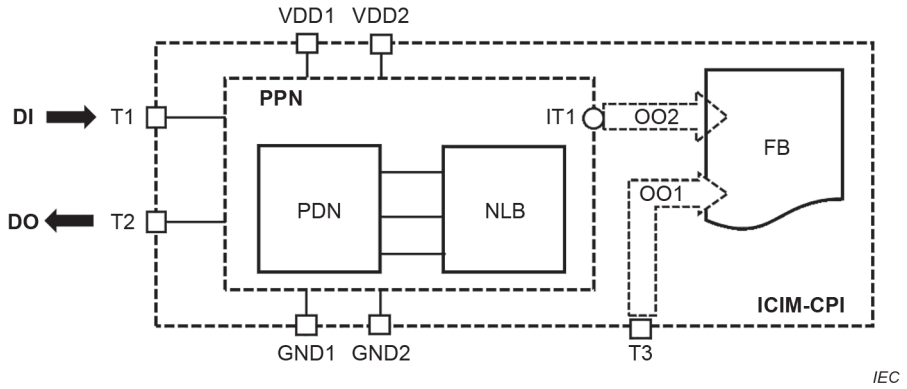

Figure 1 – Structure of the ICIM-CPI model

NOTE IT1 is an internal terminal situated within the PPN.

There is a direct electrical connection between the PDN and the NLB inside the PPN. There is no direct electrical connection between the PPN block and the FB block.

The PDN can be extracted from S-parameter measurement or design data. The NLB can be extracted from design data or from I/V measurements (using e.g. TLP) typically performed between DI and its associated external terminals (ground, power supply). The PPN can also be extracted by simulation with a circuit simulator from the design data or without simulation by processing the schematic and layout information of the IC.

The FB is a file linking the electrical characteristics in time domain of the pulse entering the DI and the electrical and/or functional characteristics measured or computed in time domain at the OO terminal. For one DI, there can be several OOs. In this case, the FB shall contain measurements or computed values performed both on a DI and its associated OOs. A failure criterion could be set on an OO to express the failure in terms of performance classes as defined in IEC 62215-3.

An ICIM-CPI model has limited validity around the conditions in which it has been extracted. Therefore, an ICIM-CPI model shall specify its validity range. Such conditions should include at least:

- power supply voltage range
- temperature range
- load conditions on the external terminals
- pulse width and pulse level

Different ICIM-CPI models can be combined to model and describe a full electronic system such as an electronic board. That proposed structure can also be used to model an equipment. The DO terminal of one ICIM-CPI model can be used to connect with the different terminals of neighbouring ICIM-CPI blocks.

Figure 2 gives a typical example of a complete ICIM-CPI model of an electronic board. The board is fully described by three stand-alone ICIM-CPI models. T11 and T21 are connected together and they receive the same disturbance. The ICIM-CPI-1 propagates a fraction of its disturbance to the ICIM-CPI-3 model through its T12 (DO) terminal which is connected to the T31 (DI) terminal of the ICIM-CPI-3 model.