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IEC 62373-1

Edition 1.0 2020-07

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Semiconductor devices – Bias-temperature stability test for metal-oxide, semiconductor, field-effect transistors (MOSFET) –
Part 1: Fast BTI test for MOSFET

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Dispositifs à semiconducteurs – Essai de stabilité de température en polarisation pour transistors à effet de champ metal-oxyde-semiconducteur (MOSFET) –
Partie 1: Essai rapide de BTI pour les MOSFET

IEC 62373-1:2020-07(en-fr)

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INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

COMMISSION
ELECTROTECHNIQUE
INTERNATIONALE

ICS 31.080.30

ISBN 978-2-8322-8610-4

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SEMICONDUCTOR DEVICES – BIAS-TEMPERATURE STABILITY TEST FOR METAL-OXIDE, SEMICONDUCTOR, FIELD-EFFECT TRANSISTORS (MOSFET) –

Part 1: Fast BTI test for MOSFET

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The text of this International Standard is based on the following documents:

FDIS	Report on voting
47/2627/FDIS	47/2637/RVD

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This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

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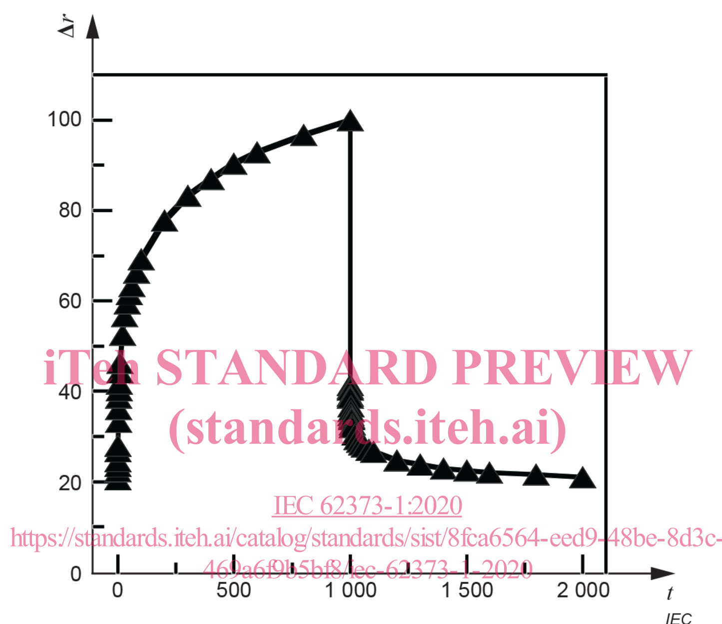
INTRODUCTION

BTI (bias temperature instability) degradation of semiconductor devices is a crucial failure. IEC 62373:2006 provides a method to test for this failure.

With advances in technology, the magnitude of recovery for BTI degradation has been remarkable. Recovery from BTI degradation occurs in microseconds to milliseconds after removing or reducing gate stress. Figure 1 below shows experiment data of V_{th} shift which is stressed in BTI condition for 1 000 s and not stressed after that [1] [1]. It shows that the degradation is rapidly recovered, to about 40 % in a few seconds right after removing the stress at 1 000 s. Therefore, a fast measurement method is necessary to avoid this effect and to determine this degradation with exactitude.



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Key

Δr ratio of V_{th} degradation amount to maximum degradation;

t stress or recovery time, expressed in seconds.

Figure 1 – Degradation (ΔV_{th}) recovering by BTI conditions removing with time

However, the existing test, described in IEC 62373, suffers from the disadvantage that the recovery process starts as soon as the stress is reduced while making the fairly lengthy set of measurements that establish the shift in threshold voltage. The procedure described in this standard uses an alternative method for measuring degradation that, by taking very little time, minimizes the partial recovery that occurs during the measurement.

1 Numbers in square brackets refer to the Bibliography.

SEMICONDUCTOR DEVICES – BIAS-TEMPERATURE STABILITY TEST FOR METAL-OXIDE, SEMICONDUCTOR, FIELD-EFFECT TRANSISTORS (MOSFET) –

Part 1: Fast BTI test for MOSFET

1 Scope

This part of IEC 62373 provides the measurement procedure for a fast BTI (bias temperature instability) test of silicon based metal-oxide semiconductor field-effect transistors (MOSFETs).

This document also defines the terms pertaining to the conventional BTI test method.

2 Normative reference

There are no normative references in this document.

3 Terms and definitions

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- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1
nominal power supply voltage
V_{DD}
suitable value of the voltage used to designate the power supply of the technology

3.2
drain – source voltage
V_{DS}
voltage between the drain and the source

3.3
gate – source voltage
V_{GS}
voltage between the gate and the source

3.4
well – source voltage
V_{BS}
voltage between the well and the source

3.5
drain current
I_D
current monitored for drain terminal when V_{BS} is zero

3.6
constant current threshold voltage
$V_{th\text{-}ci}$
V_{GS} at which drain current is equal to selected I_D

Note 1 to entry: This definition is expressed by the following equation.

$$V_{th-ci} = V_{GS}\left(\text{when } I_D = I_{D0} \times \frac{W}{L}\right) \tag{1}$$

where

$V_{th\text{-}ci}$ is constant current threshold voltage where;
I_D is drain current (arbitrary);
I_{D0} is constant value, which is recommended at $V_{GS} < V_{th\text{-}ext}$ (typically selected from 50 nA to 300 nA);
W is channel width;
L is channel length.

Note 2 to entry: If V_{GS} is over $V_{th\text{-}ext}$, it is possible that the mobility degradation affects $V_{th\text{-}ci}$ and if V_{GS} is $V_{th\text{-}ext}$, the impact of the density of interface states to V_{th} shift may not be detected.

3.7
extrapolated threshold voltage
$V_{th\text{-}ext}$
gate source voltage at which the extrapolated maximum slope of the curve of drain current versus gate source voltage intercepts the drain-current axis

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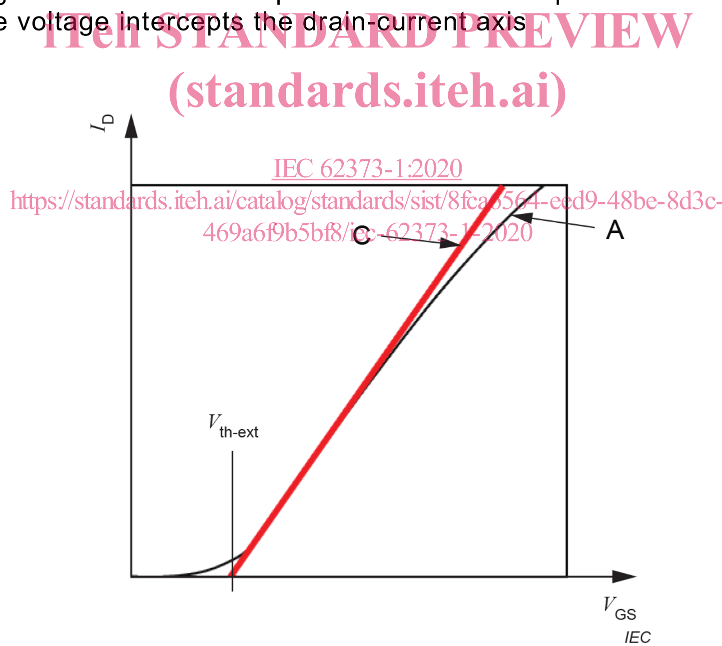
SEE: Figure 2.



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Key

A $I_D - V_{GS}$ curve;
C extrapolated maximum slope of the $I_D - V_{GS}$ curve;
$V_{th\text{-}ext}$ extrapolated threshold voltage.

Figure 2 – $I_D - V_{GS}$ curve to explain $V_{th\text{-}ext}$

3.8
saturated drain current
I_{Dsat}
drain current when the transistor is biased in the saturation region and the measure condition is $V_{DS} = V_{GS} = V_{DD}$

3.9
linear drain current
I_{Dlin}
drain current at linear region (V_{DS} = 0,05 V to 0,1 V) and $V_{GS} = V_{DD}$

3.10
gate source voltage for measurement
$V_{GS\text{-}meas}$
V_{GS} which is applied in measurement duration

3.11
drain current for measurement
$I_{D\text{-}meas}$
drain current at $V_{GS} = V_{GS\text{-}meas}$

3.12
dielectric electric field strength
E_{ox}
electric field strength in the gate dielectric

Note 1 to entry: The general formula for E_{ox} is

$$E_{ox} = \frac{V_{ox}}{t_{ox}} \quad (2)$$

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where

E_{ox} is electric field strength of gate dielectric;

V_{ox} is gate dielectric applied voltage;

t_{ox} is gate dielectric thickness.

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t_{ox} is a parameter used for inline monitoring determined by CV analysis at inversion condition. It is important to point out that the applied voltage is not necessarily the voltage across the dielectric. Ultrathin dielectrics exhibit quantum confinement effects and gate electrode depletion effects effectively reducing the voltage across the dielectric. The method of determining t_{ox} or a reference to the documented standard should be included in the data report.

4 Test equipment

4.1 Equipment

4.1.1 Wafer prober

A wafer prober equipped with a hot chuck is used. The temperature should be kept constant (within ±1 °C is recommended) during stress and measurement. All time intervals should be recorded to an accuracy of 1 %. These include the period from the first application of stress to the start of each measurement, and the duration of each measurement before the stress is re-applied.

Since some equipment is designed with a tolerance of ±3 °C, it is necessary to confirm that it is within ±1 °C by actual measurement on the chuck.

4.1.2 Measurement equipment

Measurement instruments with fast voltage switching are used for the DC characteristics of MOSFETs. The fast switching shall be in a few ms (it is recommended in a few µs, if possible). The accuracy should be maintained at high temperature.

4.2 Recommendation for handling

When it is available, it is recommended to use ESD protective equipment (wrist strap etc.) to prevent damage to the test sample.

5 Test sample

5.1 Sample

5.1.1 General

One MOSFET, as described in 5.1.2 to 5.1.5, is used.

5.1.2 Channel length (gate length)

It is recommended to use the designed minimum channel length of the targeted technology or production when individual specifications are not specifically defined, or when the minimum channel length does not yield a worse BTI. If necessary, channel length dependence may be confirmed by evaluating another channel length.

NOTE In some technologies the worst BTI is associated with the longest channel length.

5.1.3 Channel width (gate width)

The measured variability of BTI shifts is strongly dependent on the selected channel width. It is recommended to define the channel width at which the measurement is steady (see Annex B). It is better for it to be determined through pre-test. If there is no special requirement, a channel width from 1 µm to 20 µm is recommended.

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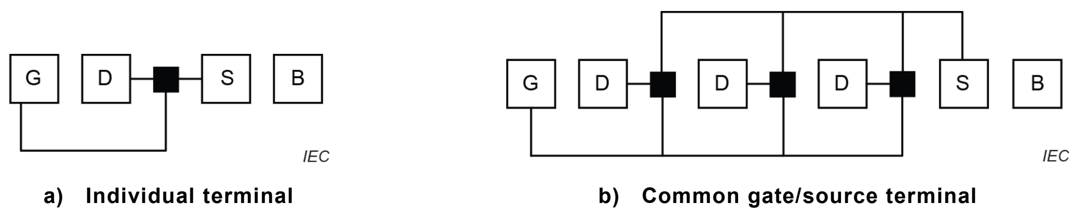
5.1.4 Structure

It is recommended that four electrodes (gate, source, drain, substrate) are connected to individual external terminals Figure 3a). A common gate/source terminal structure (see Figure 3b]) shall not be used.



a) Individual terminal b) Common gate/source terminal

Key

G gate terminal;

S source terminal;

D drain terminal;

B substrate terminal.

Figure 3 – Connection between MOSFET electrodes and external terminals

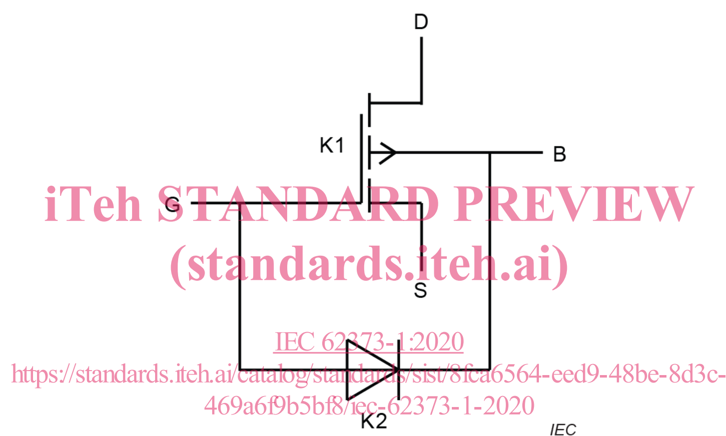
The well terminal used during stress/measurement shall be at the same bias conditions as in operation (typically V_W = 0 if bulk). To minimize parasitic voltage drops between the probe pads and the device terminals (V_{device}), the wiring resistances (R_W) from the probe pads to the device gate, source, drain, and well are selected such that the voltage drop ($I \times R_W$) is less than 1 % V_{device}.

5.1.5 Wafer process

It is strongly recommended that the steps of the wafer process, such as impurity concentration, thermal treatment, wiring process, be identical to those required by the targeted technology. The impact of process damage can be mitigated when the multi-layered metallization process is simplified for sample preparation. It is necessary to carefully consider the result.

5.2 Antenna protection diode

According to the design manual, an antenna protection diode shall be added to the gate electrode (see Figure 4) to avoid antenna damage. However, if it is necessary to consider RC delay for fast BTI measurement, unnecessary or excessive antenna protection diode should not be implemented. Drain current should be measured to an accuracy better than 0,2 %. Owing to the transient effect of switching the drain voltage, the time-constant at the input of the instrument used to measure very low levels of drain current should be taken into consideration when the measurement duration is very short. Sensitivity to possible stray voltages should also be considered.



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Key

Components		Terminals	
K1	MOSFET	G	gate terminal
K2	protection diode	S	source terminal
		D	drain terminal
		B	substrate terminal

Figure 4 – Example of antenna protection circuit for BULK process

5.3 Number of samples

Depending on the measured variability of the BTI shifts for a given device, an adequate sample size is required to achieve an assumed statistical confidence level, see Annex B. A minimum of four samples is recommended for each test condition for a large channel width (recommended in 5.1.3).