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TECHNICAL REPORT

Semiconductor devices – Scan based ageing level estimation for semiconductor devices

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SEMICONDUCTOR DEVICES –

Scan based ageing level estimation for semiconductor devices

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IEC TR 63133, which is a technical report, has been prepared by IEC technical committee 47: Semiconductor devices.

The text of this technical report is based on the following documents:

Enquiry draft	Report on voting
47/2405/DTR	47/2425/RVDTR

Full information on the voting for the approval of this technical report can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

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INTRODUCTION

A semiconductor device has an important role in reliability-critical applications, e.g., space, air and road vehicles, medical equipment. Although new technology has improved performance, power efficiency, cost efficiency etc., but the reliability becomes a serious threat [1][1]. As can be seen in Figure 1, failure rate is decreases in early life, and low constant failure rate is preserved for a while, then wear out failure rate is increases significantly. Especially for reliability-critical applications, it is important to precisely monitor the ageing level to forewarn of any impending catastrophic failure. The semiconductor ageing is caused by negative/positive bias temperature instability, hot carrier injection, and time dependent dielectric breakdown, electro migration, and stress migration, etc. Path delay is known to be increased due to various ageing failures. Although a few ageing monitoring techniques have been developed [2 to 5], the ageing level has not been precisely diagnosed. For reliability-critical applications, the ageing level information can be utilized for taking adequate measures timely, e.g., device replacement, performance switching using dynamic voltage-frequency scaling. This document describes an efficient technique to monitor the ageing and characterize the ageing level.

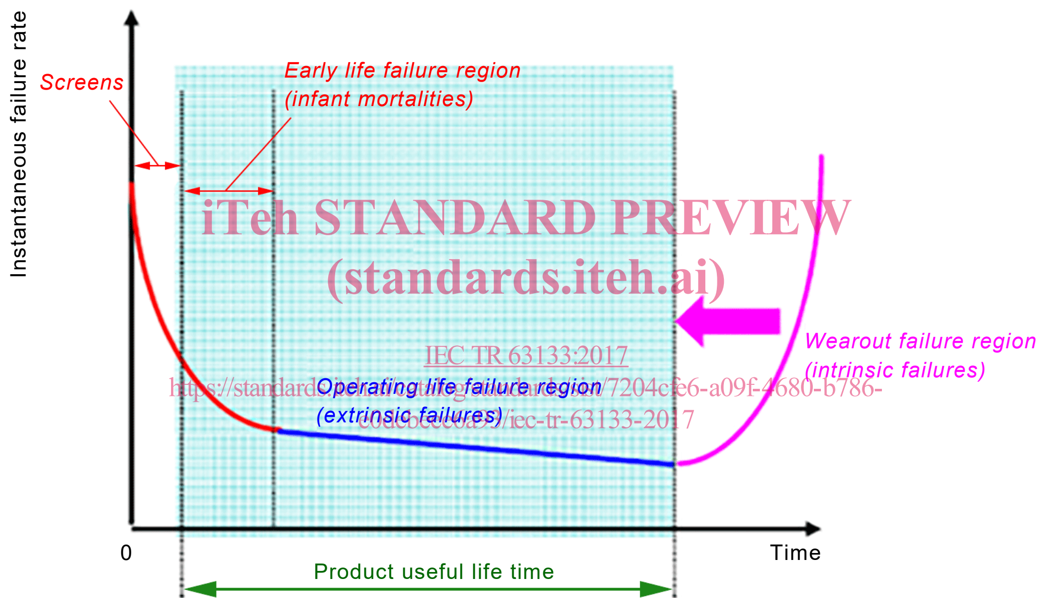

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Figure 1 – Reliability bathtub curve

1 Numbers in square brackets refer to the Bibliography.

SEMICONDUCTOR DEVICES –

Scan based ageing level estimation for semiconductor devices

1 Scope

This Technical Report specifies a design technique of performance estimation storage element, which can monitor semiconductor ageing and characterize ageing level. The estimated ageing level can be used to improve the reliability of system.

2 Normative references

There are no normative references in this document.

3 Terms, definitions and abbreviated terms

3.1 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

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ISO and IEC maintain terminological databases for use in standardization at the following addresses:

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3.1.1
transistor ageing
for a field effect transistor, increase with time of its threshold voltage

Note 1 to entry: This increase is caused by a combination of NBTI, PBTI, HCI, TDDB, EM, and SM.

Note 2 to entry: This effect decreases the drain current and transconductance and thereby increases the path delay.

3.1.2
ageing level
degree of transistor ageing under known operating conditions

3.1.3
ageing level monitoring
method of evaluating transistor ageing that indicates either pass or fail at a selected ageing level

Note 1 to entry: The amount of delay between two clock signals corresponds to the selected ageing level.

Note 2 to entry: A path delay longer than the clock delay plus guard band constitutes a failure.

3.1.4
guard band
timing margin that allows for the worst acceptable increase of path delay through a device

3.1.5
scan cell
special purpose storage element employing design-for-testability, that is used for ageing level monitoring

Note 1 to entry: A scan cell may also be used as a functional storage element when not in test mode.

3.1.6
scan chain
chain of scan cells where the output of one is the input to the next

Note 1 to entry: This type of series connection is usually called as a daisy-chain.

3.1.7
test access port
port through which test equipment may be connected

Note 1 to entry: IEEE standard 1149.1 [6] specifies four (optionally five) lines for a TAP, i.e., test data input, test data output, test mode select, test clock and an optional test reset.

3.2 Abbreviations

3.2.1

CLK

CLocK

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3.2.2

DFT

Design For Testability

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3.2.3

EM

Electro migration

3.2.4

HCI

Hot carrier injection

3.2.5

NBTI

Negative bias temperature instability

3.2.6

PBTI

Positive bias temperature instability

3.2.7

PE

Performance evaluation

3.2.8
PECLK
Performance evaluation clock

3.2.9
PERC
Performance evaluation result cell

3.2.10
PESE
Performance evaluation storage element

3.2.11
PESI
Performance evaluation SI

3.2.12
PESO
Performance evaluation SO

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3.2.13
SC
Scan cell

3.2.14
SE
Scan enable

3.2.15
SI
Scan input

3.2.16
SO
Scan output

3.2.17
SM
Stress migration

3.2.18
TAP
Test access port

3.2.19

TDDB

Time dependent dielectric breakdown

4 Ageing level

4.1 Overview

Semiconductor ageing is a serious threat to the reliability of a system. The ageing level of semiconductor components can be described as the degree of semiconductor ageing under certain operating conditions, including voltage, frequency, temperature, and usage rate. Over a certain lifetime of a semiconductor device, ageing is caused by several phenomena, including NBTI, PBTI, HCI, etc., and results in signal delay [7 to 9]. Therefore, the semiconductor ageing defect decreases the performance of a device, and ultimately causes system failure. Ageing should be precisely monitored and alarmed during functional operation for reliability. Thus, this document introduces the method to estimate the degree of ageing of a semiconductor device, in other words, the ageing-level.

4.2 Ageing level characterization technique (test method)

The ageing is modelled as a signal delay, and the ageing level can be estimated by monitoring the amount of induced delay at multiple delay points. The schematic of ageing level estimation technique can be described as in Figure 2. Normal and phase shifted clocks are applied to the device under ageing monitoring. Then the ageing level can be estimated through the ageing level analyser if any critical ageing failure is notified from the device.

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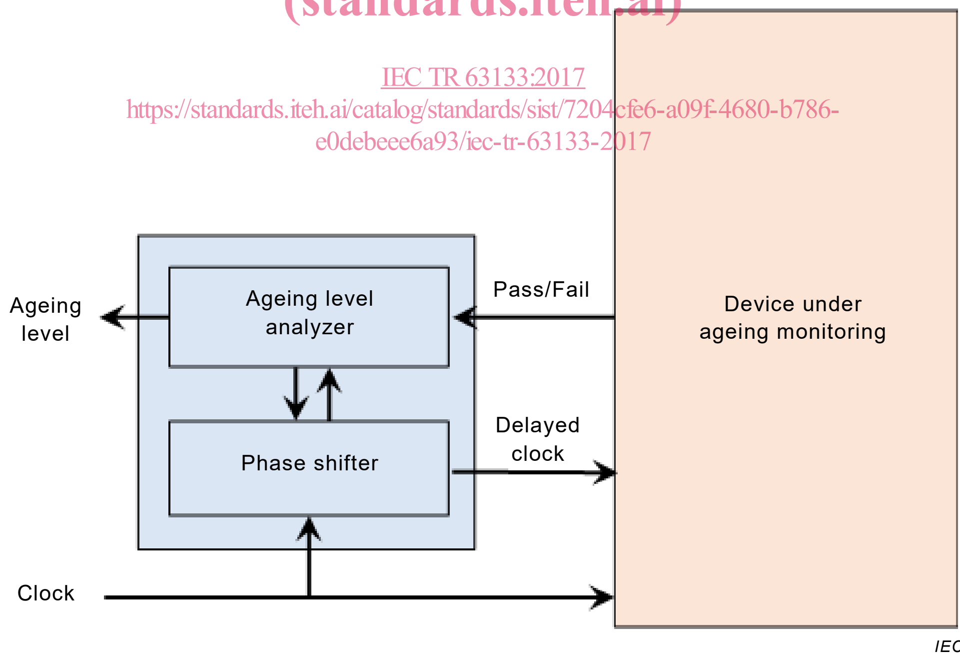

Figure 2 – Schematic of ageing level estimation technique

The monitoring range of the delay points for the ageing level is limited to the guard band as can be seen in Figure 3. The blue and red arrows indicate the ageing monitoring points representing the pass and fail in delay test, respectively. The amount of the ageing level can be estimated as the boundary value between blue and red arrows in which the delay test started to fail. As the device gets older, the ageing level becomes nearer to the rising edge of normal clock because more delay on the signal path due to the ageing causes earlier fail (red arrow) in the delay test.