

# INTERNATIONAL STANDARD

# NORME INTERNATIONALE



**Digital addressable lighting interface –  
Part 105: Particular requirements for control gear and control devices –  
Firmware transfer**

**Interface d'éclairage adressable numérique –  
Partie 105: Exigences particulières pour appareillages et dispositifs de  
commande – Transfert du microprogramme**



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INTERNATIONAL ELECTROTECHNICAL COMMISSION

**DIGITAL ADDRESSABLE LIGHTING INTERFACE –**

**Part 105: Particular requirements for control gear and control devices –  
Firmware transfer**

FOREWORD

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International Standard IEC 62386-105 has been prepared by IEC technical committee 34: Lamps and related equipment.

The text of this International Standard is based on the following documents:

FDIS	Report on voting
34/675/FDIS	34/688/RVD

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

This Part 105 of IEC 62386 is intended to be used in conjunction with:

- Part 101, which contains general requirements for system components;
- Part 102, which contains general requirements for the relevant product type (control gear), and with the appropriate Parts 2xx (particular requirements for control gear);
- Part 103, which contains general requirements for the relevant product type (control devices), and the appropriate Parts 3xx (particular requirements for control devices).

A list of all parts in the IEC 62386 series, published under the general title *Digital addressable lighting interface*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "<http://webstore.iec.ch>" in the data related to the specific document. At this date, the document will be

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- withdrawn,
- replaced by a revised edition, or
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## INTRODUCTION

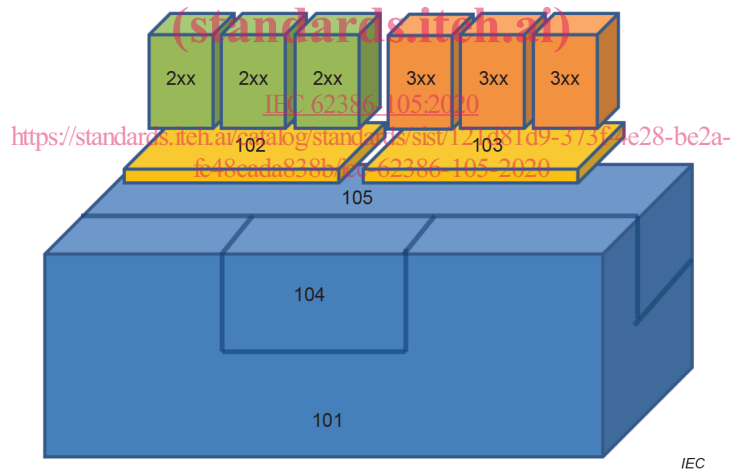
IEC 62386 contains several parts, referred to as series. The IEC 62386 series specifies a bus system for control by digital signals of electronic lighting equipment. The IEC 62386-1xx series includes the basic specifications. Part 101 contains general requirements for system components, Part 102 extends this information with general requirements for control gear and Part 103 extends it further with general requirements for control devices.

The IEC 62386-2xx series extends the general requirements for control gear with lamp specific extensions (mainly for backward compatibility with Edition 1 of IEC 62386) and with control gear specific features.

The IEC 62386-3xx series extends the general requirements for control devices with input device specific extensions describing the instance types as well as some common features that can be combined with multiple instance types.

This first edition of IEC 62386-105 is intended to be used in conjunction with IEC 62386-101, IEC 62386-102 and the various parts that make up the IEC 62386-2xx series for control gear, together with IEC 62386-103 and the various parts that make up the IEC 62386-3xx series of particular requirements for control devices. The division into separately published parts provides for ease of future amendments and revisions. Additional requirements will be added as and when a need for them is recognized.

The setup of the standards is graphically represented in Figure 1 below.



**Figure 1 – IEC 62386 graphical overview**

When this part of IEC 62386 refers to any of the clauses of the IEC 62386-1xx series, the extent to which such a clause is applicable and the order in which the tests are to be performed are specified. The other parts also include additional requirements, as necessary.

All numbers used in this document are decimal numbers unless otherwise noted. Hexadecimal numbers are given in the format 0xVV, where VV is the value. Binary numbers are given in the format XXXXXXXXb or in the format XXXX XXXX, where X is 0 or 1, "x" in binary numbers means "don't care".

The following typographic expressions are used:

Variables: *variableName* or *variableName*[3:0], giving only bits 3 to 0 of *variableName*

Range of values: [lowest, highest]

Command: "COMMAND NAME"



## DIGITAL ADDRESSABLE LIGHTING INTERFACE –

### Part 105: Particular requirements for control gear and control devices – Firmware transfer

#### 1 Scope

This part of IEC 62386 applies to control gear and control devices.

Typically, a bus unit according to IEC 62386 (all parts) contains firmware. There are circumstances where it might be necessary to change the firmware after production or shipping of the product. For example if the bus unit does not operate as intended. In such a case, a firmware update of a bus unit via the interface is beneficial.

This firmware update process is primarily designed to be a bug fix process, not a feature extension process. Nevertheless the firmware update process can be used for feature extensions. But it is important that the risk of negative effects to the complete system is considered in detail.

NOTE Annex D provides a “Firmware update management check sheet” to support risk estimation.

#### 2 Normative references (standards.iteh.ai)

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 62386-101:2014, *Digital addressable lighting interface – Part 101: General requirements – System components*  
IEC 62386-101:2014/AMD1:2018

IEC 62386-102:2014, *Digital addressable lighting interface – Part 102: General requirements – Control gear*  
IEC 62386-102:2014/AMD1:2018

IEC 62386-103:2014, *Digital addressable lighting interface – Part 103: General requirements – Control devices*  
IEC 62386-103:2014/AMD1:2018

#### 3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 62386-101, IEC 62386-102 and IEC 62386-103 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at <http://www.electropedia.org/>
- ISO Online browsing platform: available at <http://www.iso.org/obp>

### **3.1 firmware FW**

software programmed into a control gear or control device, which can be changed during an update

Note 1 to entry: This note applies to the French language only.

### **3.2 CRC cyclic redundancy check**

checksum used to prevent data corruption

Note 1 to entry: Annex B provides detailed information about CRC calculation.

## **4 General**

### **4.1 General**

The requirements of IEC 62386-101:2014 and IEC 62386-101:2014/AMD1:2018 apply, with the restrictions, changes and additions identified below.

NOTE Systems with a single-master application controller are unlikely to operate correctly when other master control devices, such as upgrade tools, are connected.

### **4.2 Transmitters and receivers in bus units**

The requirements of IEC 62386-101:2014 and IEC 62386-101:2014/AMD1:2018, 4.6.1 shall be extended as follows.

Bus units supporting firmware transfer shall be additionally capable of receiving 32 bit forward frames as specified in IEC 62386-101:2014 7.4.3 (Reserved forward frame).

### **4.3 Logical units in a bus unit**

If the firmware update process is started on a bus unit, all logical units inside the bus unit shall be affected. All variables defined in Table 5 shall be shared by all logical units of the bus unit.

## **5 Electrical specification**

The requirements of IEC 62386-101:2014 and IEC 62386-101:2014/AMD1:2018, Clause 5 apply.

## **6 Interface power supply**

The requirements of IEC 62386-101:2014 and IEC 62386-101:2014/AMD1:2018, Clause 6 apply.

## **7 Transmission protocol structure**

### **7.1 General**

The requirements of IEC 62386-101:2014, Clause 7 apply, with the following additions.

## 7.2 32 bit forward frame encoding

The forward frame format used for firmware update consists of  $n = 32$  data bits as described in IEC 62386-101:2014, 7.4.3 (Reserved forward frame).

The 32 bit forward frame for 32 bit frames shall be encoded as shown in Table 1.

**Table 1 – 32-bit command frame encoding**

Bytes/Bits								Device addressing method			
Address byte							Opcode byte				
31	30	29	28	27	26	25	24 <sup>a</sup>	23...16	15...8	7...0	
0	64 short addresses						x				Short addressing
1	1	1	1	1	1	0	x			Broadcast unaddressed	
1	1	1	1	1	1	1	x			Broadcast	
All other address byte values.										Reserved	

<sup>a</sup> For bit 24, 0 indicates address space for control gear, 1 indicates address space for control devices.

## 8 Timing

The requirements of IEC 62386-101:2014 and IEC 62386-101:2014/AMD1:2018, Clause 8 apply.

## 9 Method of operation

### 9.1 General

The requirements of IEC 62386-101:2014 and IEC 62386-101:2014/AMD1:2018, 9.8 (Dealing with frames and commands), 9.2 (Transactions) with the exception that the total duration may exceed 400 ms, 9.4 (Command iteration) and 9.6 (Use of multiple bus power supplies) apply.

### 9.2 Data transmission

A bus unit receives a new FW block by block. The first block (block 0) contains information about the type of bus unit (see Table 3), which receives a new FW. This avoids transferring the wrong FW to a bus unit if more than one bus unit is updated at a time.

NOTE Annex A provides detailed information about the update file.

The opcode byte 1 shall be 0xFB for 32-bit standard commands (see Table 6). If the opcode byte 1 in a standard command is not equal to 0xFB, the bus unit shall not accept the standard command.

### 9.3 Duration

A data transmission frame consists of a start bit, 32 data bits and a stop condition, which occupies the bus for around 30 ms. With a settling time of less than 15 ms (maximum frame priority) the transmission of three bytes takes less than 45 ms. For an update of 64 kByte it is expected to take less than 20 min.

## 9.4 Security

It is recommended that the individual manufacturer ensures firmware image integrity and authenticity. This document specifies the use of CRC checksums to help ensure error-free transfer of data.

## 9.5 Firmware update features

Each bus unit shall expose its firmware update features as a combination of device properties as given in Table 2.

**Table 2 – Firmware update features**

Bit	Description	Value	See
0	" <i>fwUpdateCancelSupported</i> " is TRUE?	"1" = "YES"	XXX
1-7	Reserved – not implemented	"0" = "NO"	

The bus unit firmware update features can be queried using QUERY FW UPDATE FEATURES.

If the bus unit supports cancellation of the firmware update process (see 9.6.2.3), "*fwUpdateCancelSupported*" is set to TRUE.

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## 9.6 Update process

### 9.6.1 Start firmware update

A bus unit shall enable the firmware update process by the acceptance of the command START FW TRANSFER. Several bus units can be addressed in this way to update more than one bus unit at a time.

NOTE 1 Annex C provides an example of the firmware update process.

It is recommended not to trigger erasing of the memory before block 0 is verified.

Whilst "*fwUpdateProcessEnabled*" is TRUE, the operation of the bus unit is manufacturer-specific except for the requirements given in this document.

NOTE 2 This includes, for example, the reaction to commands of other parts of the IEC 62386 series.

### 9.6.2 Data transfer

#### 9.6.2.1 Block 0 (information block)

Block 0 contains all data for the bus unit to decide if it will accept the new firmware or not.

The GTIN number, the hardware version number and the firmware version number contained in the bus unit are described in IEC 62386-102:2014 and IEC 62386-102:2014/AMD1:2018, 9.10.6 (Memory bank 0 for control gear) and IEC 62386-103:2014 and IEC 62386-103:2014/AMD1:2018, 9.10.6 (Memory bank 0 for control devices). A bus unit shall have a maximum of one family GTIN which shall be shown in the documentation of the bus unit.

Upon reception of a complete block 0, the following information is checked, where Table 3 shows block 0 content:

- The received block 0 "Size of block" is equal to the value shown in Table 3.
- The received block 0 "Block 0 version" is equal to the value shown in Table 3.

- The received block 0 “GTIN” matches the GTIN stored in memory bank 0.
- (Received block 0 “FW version min”) ≤ (memory bank 0, Firmware version) ≤ (received block 0 “FW version max”).
- (Received block 0 “HW version min”) ≤ (memory bank 0, Hardware version) ≤ (received block 0 “HW version max”).
- (Received block 0 “Identification number min”) ≤ (memory bank 0, Identification number) ≤ (received block 0 “Identification number max”).
- The received block 0 “Device key” meets manufacturer-specific requirements.
- The received block 0 “CRC” matches the calculated value based on the block 0 content (see Annex B).

If the above check is successful, the following operation shall result:

- “*sessionKey*” shall be set to the received block 0 “Session key”,
- “*currentBlock*” shall be set to 1,
- “*currentBlockByte*” shall be set to 0,
- previously received block data that is unwritten, may be discarded.

Otherwise, the following operation shall result:

- “*fwUpdateProcessEnabled*” shall be set to FALSE and resume normal operation if possible.

**Table 3 – Block 0 definitions**

Address (hex)	Size (bytes)	Description
00	1	Size of block (fixed value of 0x3D for block 0)
01	1	Block 0 version (always 0x00)
02..04	3	Total block count (MSB first) <sup>a</sup>
05..0A	6	GTIN (MSB first)
0B..0C	2	HW version min (MSB first)
0D..0E	2	HW version max (MSB first)
0F..10	2	FW version min (MSB first)
11..12	2	FW version max (MSB first)
13..1A	8	Identification number min (MSB first)
1B..22	8	Identification number max (MSB first)
23..2A	8	Session key <sup>b</sup>
2B..3A	16	Device key <sup>c</sup>
3B..3C	2	CRC (MSB first)

<sup>a</sup> This is the amount of blocks being transferred during the firmware update.

<sup>b</sup> The session key is generated by the bus unit, which transfers the firmware update.

<sup>c</sup> The device key and its use is manufacturer-specific. It allows the manufacturer to specify different areas/options in his firmware.

It is recommended to calculate the CRC checksums with the incoming bytes to minimize delay at the end of the block reception.

### 9.6.2.2 Block 1..n (data block)

A bus unit shall only accept a block, if the following condition is true:

- “*fwUpdateProcessEnabled*” is TRUE, and

- The session key matches the received block 0 "Session key".

After reception of a whole block, the consistency of the firmware data inside the block shall be verified by CRC (address 0D...0E). The data consistency of the whole block shall be verified by a second CRC (address s+0F...s+10). If the verification fails, the bus unit shall discard the block. If a block is valid, but is the same as the last programmed block, it is recommended to discard the block to prevent unnecessary write cycles.

**Table 4 – Block 1..n definitions**

Address (hex)	Size (bytes)	Description
00..01	2	s = Size of block data bytes (MSB first)
02..09	8	Session key
0A..0C	3	Block number (MSB first)
0D..0E	2	CRC (of block data bytes)
0F..(s+0E)	s	Firmware data (optionally encrypted by manufacturer)
s+0F..s+10	2	CRC (of total block)
NOTE This allows a theoretical maximum of 65 535 bytes of firmware data per block, resulting in a maximum total of 65 552 bytes in the block.		

It is recommended to calculate the CRC checksums with the incoming bytes to minimize delay at the end of the block reception.



**9.6.2.3 Cancel firmware update**

If a bus unit physically supports cancellation of FW updates and can return to the previous FW, the bus unit shall respond to QUERY FW UPDATE FEATURES with 0000001b.

If a bus unit supports cancellation of the FW updates, the bus unit shall set "*fwUpdateProcessEnabled*" to FALSE by the acceptance of the command CANCEL FW UPDATE.

If a bus unit physically does not support a cancellation of the FW update process, it shall ignore this command.

**9.6.3 Persistent variables during firmware update**

A firmware update may totally change the internal structure of the corresponding bus unit.

The values for

- the GTIN,
- the identification number,
- the hardware version,

shall not be affected by a firmware update.

If a bus unit operates in the standard mode described as operating mode 0x00 in IEC 62386-102:2014 and IEC 62386-102:2014/AMD1:2018, 9.10 for control gear and in IEC 62386-103:2014 and IEC 62386-103:2014/AMD1:2018, 9.10.5 for control devices, each NVM variable shall either remain unchanged or be set to factory default as a result of a firmware update. The short addresses of all logical units shall be maintained at least until the firmware update successfully completes. For a bus unit in an operating mode different from 0x00, the variables do not need to be in factory default state.

The manufacturer shall provide a document stipulating which variables are affected by the update and if a re-commissioning of the system is necessary after the firmware update process.

After a firmware update, an updated bus unit should first proceed to a power up sequence to (re-)load RAM variables.

It is recommended that all NVM variables remain unchanged as a result of the firmware update.

NOTE Due to the fact that the programme memory of a bus unit is updated, values in other parts of the IEC 62386 series marked as ROM can be changed.

#### 9.6.4 Firmware version number

It is allowed to transfer the same firmware to a bus unit multiple times using this procedure.

It is strongly recommended that two firmware update files containing different firmware do not contain the same GTIN number and the same firmware version number.

#### 9.6.5 Firmware update in a system

If "*fwUpdateProcessEnabled*" is TRUE, it is permitted that the bus unit discards some or all commands not described in this document (see 11.3.1).

It is recommended to run the firmware update under human observation to be able to react to occurring errors.

It is recommended to avoid communication on the bus while a firmware update process is running.

<https://standards.itech.ai/catalog/standards/sist/121d81d9-373f-4e28-be2a-fc48cada838b/iec-62386-105-2020>

NOTE The device executing the firmware update can use the quiescent mode defined in IEC 62386-103:2014 and IEC 62386-103:2014/AMD1:2018, 9.10.4, to suppress forward frames from other bus units.

#### 9.6.6 Error recovery

If a bus unit is prevented from completing the firmware update by a temporary event such as power failure or communications interruption, it shall be possible to re-establish and complete the firmware update process over the bus.

EXAMPLE An example implementation would be a "bootloader". The bootloader is a smaller partitioned piece of firmware that is capable of communicating over the bus and implementing the download and programming of a new firmware. If the bootloader does not complete the firmware update it will retain control until the process is re-established and completed. A common method is to start again from the beginning.

NOTE If a firmware update process is started, some or all other commands can be stopped from execution.

## 10 Declaration of variables

Additional variables are given in Table 5.