

# INTERNATIONAL STANDARD

## NORME INTERNATIONALE

**Mechanical standardization of semiconductor devices –  
Part 6-6: General rules for the preparation of outline drawings of surface  
mounted semiconductor device packages – Design guide for fine pitch land grid  
array (FLGA)**

[IEC 60191-6-6:2001](https://standards.iteh.ai/catalog/standards/sist/23ef94d0-abb9-40fb-9ea6-)

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**Normalisation mécanique des dispositifs à semiconducteurs –  
Partie 6-6: Règles générales pour la préparation des dessins d'encombrement  
des dispositifs à semiconducteurs à montage en surface – Guide de conception  
des dispositifs FLGA**



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INTERNATIONAL ELECTROTECHNICAL COMMISSION

**MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –**

**Part 6-6: General rules for the preparation of outline drawings  
of surface mounted semiconductor device packages –  
Design guide for fine-pitch land grid array (FLGA)**

FOREWORD

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International Standard IEC 60191-6-6 has been prepared by subcommittee 47D: Mechanical standardization of semiconductor devices, of IEC technical committee 47: Semiconductor devices.

This bilingual version (2013-01) corresponds to the monolingual English version, published in 2001-03.

The text of this standard is based on the following documents:

FDIS	Report on voting
47D/404/FDIS	47D/421/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

The French version of this standard has not been voted upon.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 3.

The committee has decided that the contents of this publication will remain unchanged until 2003. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

## INTRODUCTION

The demand for area array style packages exists because of the multi-functions and high performance of electrical equipment. The objective of this design guide is to standardize outlines and to get interchangeability of FLGA packages. The terminal pitch and package outlines of these fine-pitch array packages are smaller than those of LGA packages.

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## MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

### Part 6-6: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for fine-pitch land grid array (FLGA)

#### 1 Scope

This part of IEC 60191 provides common outline drawings and dimensions for all types of structures and composed materials of fine-pitch land grid array (hereinafter called FLGA) whose terminal pitch is less than, or equal to, 0,80 mm and whose package body outline is square.

#### 2 Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this part of IEC 60191. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this part of IEC 60191 are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies. Members of IEC and ISO maintain registers of currently valid International Standards.

IEC 60191 (all parts), *Mechanical standardization of semiconductor devices*  
[IEC 60191-6-6:2001](#)

#### 3 Definitions

<https://standards.iteh.ai/catalog/standards/sist/23e94d0-abb9-40fb-9ea6-f70169b7398d/iec-60191-6-6-2001>

For the purposes of this part of IEC 60191, the following definitions, as well as those given in the other parts of this standard, apply.

##### 3.1

##### **flanged type**

type whose package body size (body length and width) consists of its own flange composed around the encapsulation or lid

##### 3.2

##### **type of real chip size**

type whose package body size (body length and width) consists of an encapsulation around the real chip only

##### 3.3

##### **FLGA**

packages with metal lands or metal bumps of which the terminal height is less than, or equal to, 100  $\mu\text{m}$ , and whose terminal pitch is less than, or equal to, 0,80 mm, positioned in an array on the base plane of the package as external terminals

This package structure makes it possible to surface-mount the packages to the printed circuit board

### **3.4**

#### **material designation**

FLGA packages are classified according to the following two material designations:

#### **3.4.1**

##### **plastic type (P-FLGA)**

plastic-type classification is assigned to packages which consist of resin substrate as interposer material (for example, glass-epoxy, poly-imid)

#### **3.4.2**

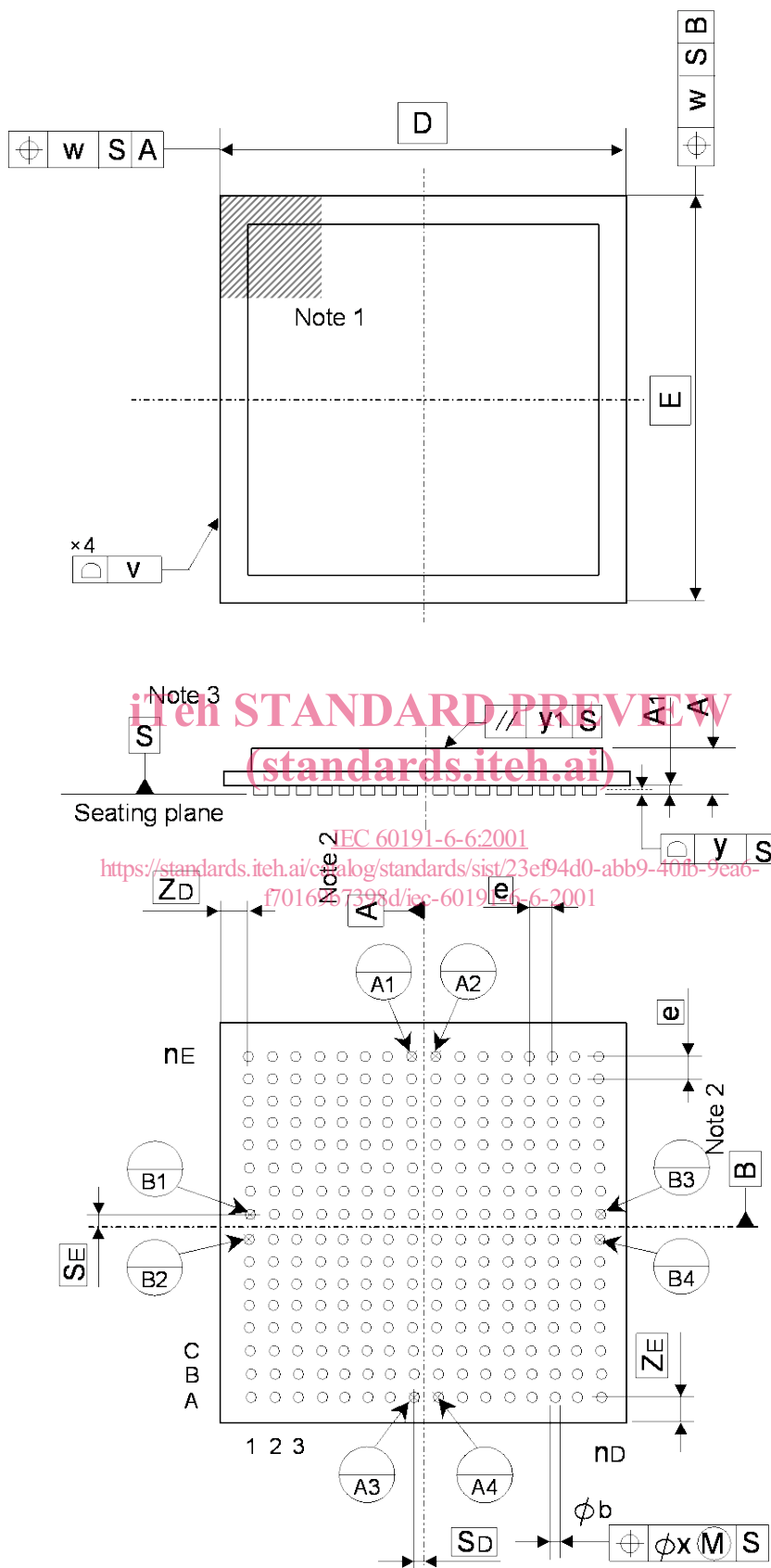
##### **ceramic type (C-FLGA)**

ceramic-type classification is assigned to packages which consist of ceramic substrate as interposer material

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IEC 300/01

**Design guide for  
fine-pitch land grid array family**

**IEC 60191**



NOTE 1 Zone of a visible index on the top surface.

NOTE 2 Datum A and B are the axes defined by the terminal positions indicated with datum targets.

NOTE 3 Primary datum S and seating plane to be defined by the method of least squares of spherical crowns of terminals.

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**Table 1 – Group 1: Dimensions appropriate to mounting and interchangeability**

Ref.	Limits to be observed			Recommended values for the dimensions mm	Note																																								
	Min.	Nom.	Max.																																										
n		X			1, 2																																								
nD		X			1																																								
nE		X																																											
A			X	A max. = 1,20, 1,70, 2,00	Includes heat slug Includes package warpage and tilt																																								
A <sub>1</sub>			X	A <sub>1</sub> max. = 0,10																																									
∅b	X	X	X	At ceramic FLGA (C-FLGA) <table border="1"> <thead> <tr> <th></th> <th>Min.</th> <th>Nom.</th> <th>Max.</th> </tr> </thead> <tbody> <tr> <td>at e = 0,80</td> <td>0,45</td> <td>0,50</td> <td>0,55</td> </tr> <tr> <td>at e = 0,65</td> <td>0,35</td> <td>0,40</td> <td>0,45</td> </tr> <tr> <td>at e = 0,50</td> <td>0,25</td> <td>0,30</td> <td>0,35</td> </tr> <tr> <td>at e = 0,40</td> <td>0,20</td> <td>0,25</td> <td>0,30</td> </tr> </tbody> </table> At plastic FLGA (P-FLGA) <table border="1"> <thead> <tr> <th></th> <th>Min.</th> <th>Nom.</th> <th>Max.</th> </tr> </thead> <tbody> <tr> <td>at e = 0,80</td> <td>0,35</td> <td>0,40</td> <td>0,45</td> </tr> <tr> <td>at e = 0,65</td> <td>0,28</td> <td>0,33</td> <td>0,38</td> </tr> <tr> <td>at e = 0,50</td> <td>0,20</td> <td>0,25</td> <td>0,30</td> </tr> <tr> <td>at e = 0,40</td> <td>0,15</td> <td>0,20</td> <td>0,25</td> </tr> </tbody> </table>		Min.	Nom.	Max.	at e = 0,80	0,45	0,50	0,55	at e = 0,65	0,35	0,40	0,45	at e = 0,50	0,25	0,30	0,35	at e = 0,40	0,20	0,25	0,30		Min.	Nom.	Max.	at e = 0,80	0,35	0,40	0,45	at e = 0,65	0,28	0,33	0,38	at e = 0,50	0,20	0,25	0,30	at e = 0,40	0,15	0,20	0,25	
	Min.	Nom.	Max.																																										
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at e = 0,50	0,20	0,25	0,30																																										
at e = 0,40	0,15	0,20	0,25																																										
D		X		At flanged type D = 4,0, 5,0, 6,0, 7,0, 8,0, 9,0, 10,0, 11,0, 12,0, 13,0, 14,0, 15,0, 16,0, 17,0, 18,0, 19,0, 20,0, 21,0 At type of real chip size D = from 3,1 to 21,0	Dimension range shows nominal value																																								
E		X		At flanged type E = 4,0, 5,0, 6,0, 7,0, 8,0, 9,0, 10,0, 11,0, 12,0, 13,0, 14,0, 15,0, 16,0, 17,0, 18,0, 19,0, 20,0, 21,0 At type of real chip size E = from 3,1 to 21,0	Dimension range shows nominal value																																								
e		X		e = 0,80, 0,65, 0,50, 0,40																																									
v			X	v = 0,15	Includes burrs																																								
w			X	at e = 0,80 w = 0,20 at e = 0,65 w = 0,20 at e = 0,50 w = 0,20 at e = 0,40 w = 0,15																																									
x			X	at e = 0,80 x = 0,08 at e = 0,65 x = 0,08 at e = 0,50 x = 0,05 at e = 0,40 x = 0,05																																									

Table 1 – (continued)

Ref.	Limits to be observed			Recommended values for the dimensions mm	Note
	Min.	Nom.	Max.		
y			X	at e = 0,80 y = 0,10 at e = 0,65 y = 0,10 at e = 0,50 y = 0,08 at e = 0,40 y = 0,08	
y <sub>1</sub>			X	y <sub>1</sub> = 0,2	
NOTE 1 The values stipulated by the mathematical expression should be applied to the individual overall dimensional standards.					
NOTE 2 Symbol n refers to the total number of terminal positions.					

Table 2 – Group 2: Dimensions appropriate to mounting and gauging

Ref.	Limits to be observed			Recommended values for the dimensions mm	Note
	Min.	Nom.	Max.		
∅b <sub>2</sub>			X	At ceramic FLGA (C-FLGA) at e = 0,80 b <sub>2</sub> = 0,63 at e = 0,65 b <sub>2</sub> = 0,53 at e = 0,50 b <sub>2</sub> = 0,40 at e = 0,40 b <sub>2</sub> = 0,35 At plastic FLGA (P-FLGA) at e = 0,80 b <sub>2</sub> = 0,53 at e = 0,65 b <sub>2</sub> = 0,46 at e = 0,50 b <sub>2</sub> = 0,35 at e = 0,40 b <sub>2</sub> = 0,30	
$\boxed{e}$		X		e = 0,80, 0,65, 0,50, 0,40	
$\boxed{eD}$		X		eD = e x (nD – 1)	1 <sup>a</sup>
$\boxed{eE}$		X		eE = e x (nE – 1)	
<sup>a</sup> See note 1 of table 1.					

**Table 3 – Group 3: Dimensions appropriate to automated handling**

Ref.	Limits to be observed			Recommended values for the dimensions mm	Note
	Min.	Nom.	Max.		
A			X	A max. = 1,20, 1,70, 2,00	Includes heat slug Includes package warpage and tilt
$\overline{D}$ $\overline{E}$ $y_1$		X  X	  X	D/E = 4,0, 5,0, 6,0, 7,0, 8,0, 9,0, 10,0, 11,0, 12,0, 13,0, 14,0, 15,0, 16,0, 17,0, 18,0, 19,0, 20,0, 21,0  $y_1 = 0,2$	

**Table 4 – Group 4: Dimensions for information only**

Ref.	Limits to be observed			Recommended values for the dimensions mm	Note
	Min.	Nom.	Max.		
$\overline{ZD}$ $\overline{ZE}$		X X		$ZD = (D - e \times (nD - 1))/2$ $ZE = (E - e \times (nE - 1))/2$	1 <sup>a</sup>
<sup>a</sup> See note 1 of table 1.					

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