

TECHNICAL SPECIFICATION



**Nanomanufacturing – Key Control Characteristics –
Part 8-3: Nano-enabled metal-oxide interfacial devices – Analogue resistance
change and resistance fluctuation: Electrical resistance measurement**

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

**NANOMANUFACTURING –
KEY CONTROL CHARACTERISTICS –**

**Part 8-3: Nano-enabled metal-oxide interfacial devices –
Analogue resistance change and resistance fluctuation:
Electrical resistance measurement**

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IEC TS 62607-8-3 has been prepared by IEC technical committee 113: Nanotechnology standardization for electrical and electronic products and systems. It is a Technical Specification.

The text of this Technical Specification is based on the following documents:

Draft	Report on voting
113/743/DTS	113/767/RVDTS

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this Technical Specification is English.

A list of all parts in the IEC 62607 series, published under the general title *Nanomanufacturing – Key control characteristics*, can be found on the IEC website.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

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INTRODUCTION

Nano-enabled metal-oxide interfaces, such as an oxide nanolayer sandwiched by metal electrodes, are the essential components of IoT devices for computing. Nano-enabled functions derived from the nanoscale metal-oxide interface and the oxide nanolayer appear, such as a significant change in electrical resistance. The analogue resistance change is the typical characteristic which possesses the large potential for non-von Neumann information processing. More concretely, the metal-oxide interfacial device is an indispensable element in the product-sum circuit that records the learning process as the analogue resistance change. In the research community, however, the analogue change and the fluctuation of the resistance have not yet been systematically investigated. The reason why systematic research and development is not progressing is that the measurement protocol of these characteristics is not quantitative. The bottleneck impedes not only the electrotechnical evaluation of the device but also developments for various applications.

This document offers a measurement protocol of the analogue resistance change and the quantitative index to evaluate the linearity of the analogue resistance change in nano-enabled metal-oxide interfacial devices.

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NANOMANUFACTURING – KEY CONTROL CHARACTERISTICS –

Part 8-3: Nano-enabled metal-oxide interfacial devices – Analogue resistance change and resistance fluctuation: Electrical resistance measurement

1 Scope

This part of IEC 62607, which is a Technical Specification, specifies a measurement protocol to determine the key control characteristics

- analogue resistance change, and
- resistance fluctuation

for nano-enabled metal-oxide interfacial devices by

- electrical resistance measurement.

Analogue resistance change as a function of applied voltage pulse is measured in metal-oxide interfacial devices. The linearity in the relationship of the variation of conductance and the pulse number is evaluated using the parameter fitting. The parameter of the resistance fluctuation is simultaneously computed in the fitting process.

- This method is applicable for evaluating computing devices composed of the metal-oxide interfacial device, for example, product-sum circuits, which record the learning process as the analogue resistance change.

2 Normative references

[IEC TS 62607-8-3:2023](https://standards.iteh.ai/catalog/standards/iec/446c0464-5203-4045-a216-5d7e2120bcf2/iec-ts-62607-8-3-2023)

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The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO 80004-1, *Nanotechnologies – Vocabulary – Part 1: Core vocabulary*

3 Terms, definitions, acronyms, and abbreviated terms

3.1 Terms and definitions

For the purposes of this document, the terms and definitions given in ISO 80004-1 and the following apply.

ISO and IEC maintain terminological databases for the use in standardization at the following addresses:

- IEC Electropedia: available at <http://www.electropedia.org/>
- ISO Online browsing platform: available at <http://www.iso.org/obp>

3.1.1

device under test

DUT

sample attached to an apparatus for evaluation of a specific physical property such as electrical resistance or I - V behaviour

3.1.2

DC, qualifier

pertaining to time-independent electric quantities such as voltage or current, to devices operated with direct voltage and current, or to quantities associated with these devices

Note 1 to entry: The notation "DC" is preferred in English to the notation "d.c." which is an abbreviation of "direct current".

[SOURCE: IEC 60050-151:2001, 151-15-02, modified – Notes 2, 3 and 4 to entry have been deleted.]

3.2 Terms specific to this document

3.2.1

analogue resistance change

continuous variation of resistance as a function of applied voltage pulse

Note 1 to entry: When a voltage is applied to a metal-oxide interfacial device, for example, a resistive memory device, the resistance increases or decreases in an analogue manner based on the sign of the voltage [1].

Note 2 to entry: This kind of resistive device can be used to mimic a neural synapse wherein the resistance acts like a weight that modulates the voltage applied to it [1].

3.2.2

resistance fluctuation

least-squares error obtained during parameter fitting of analogue resistance changes

3.3 Abbreviated terms

SMU source measure unit

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4 Measurement of resistance

4.1 General

The reliable test protocol of analogue resistance measurement is standardized. A schematic diagram of the typical resistance measurement is shown in Figure 1. Figure 2 is a set of example photos showing how the DUT is set onto a sample stage.

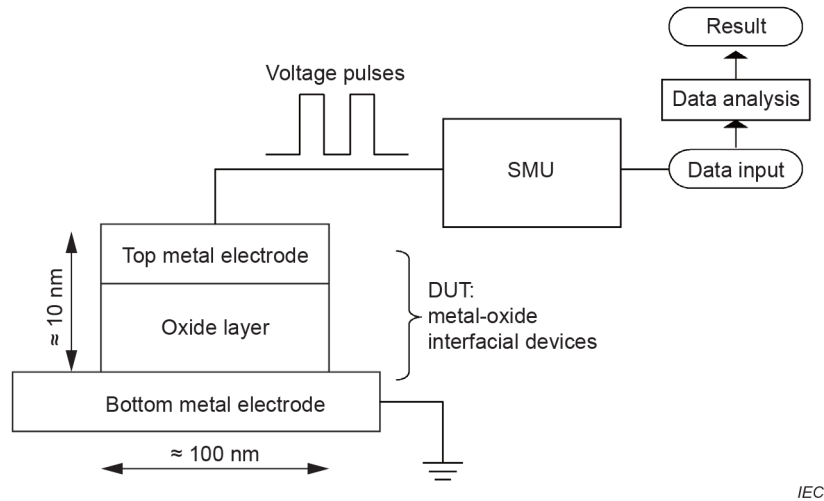
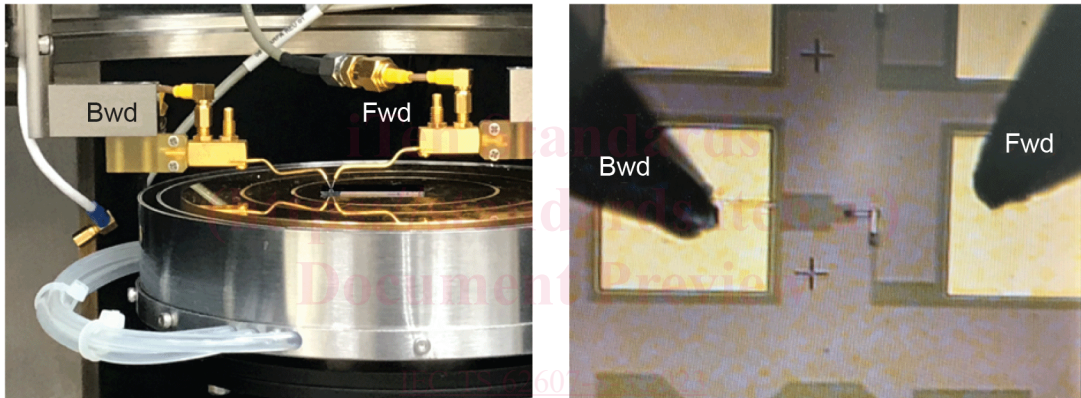


Figure 1 – Example of the experimental schematic diagram for the resistance measurement



Forward (Fwd) and backward (Bwd) contacts are shown.

Figure 2 – Photos of the sample stage

4.2 Method for processing and fabrication of DUT

Report the stacking structure of DUT, such as the material and the thickness of the metal-oxide interfacial device. In addition, the fabrication process information is important to be reported, such as the method of deposition, the shape of the DUT, and the electronic contact to SMU.

In order to avoid resistance measurement artifacts, the electric resistance of the substrate (R_{sub}) should be higher than that of the DUT (R_{dut}). The parallel current path in the substrate becomes smaller with the ratio of R_{dut}/R_{sub} . This value should be smaller than the error bar of the data. The electronic contact resistance, for example between the contact pad and the probe, should be minimized.

4.3 Experimental procedures

- Step 1. Recording of measurement conditions: temperature, humidity, and measurement setup, such as the probe specifications.
- Step 2. Sample setting: the DUT is mounted on the stage to connect to SMU electrically.
- Step 3. DC I - V measurement: from the result of DC I - V measurement, the ranges of current and voltage sweeps are decided.