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INTERNATIONAL STANDARD

NORME INTERNATIONALE

Circuit boards and circuit board assemblies – Design and use – Part 6-1: Land pattern design – Generic requirements for land pattern on circuit boards

Cartes imprimées et cartes imprimées équipées – Conception et utilisation – Partie 6-1: Conception de la zone de report – Exigences génériques pour la zone de report sur les cartes imprimées

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CIRCUIT BOARDS AND CIRCUIT BOARD ASSEMBLIES – DESIGN AND USE –

Part 6-1: Land pattern design – Generic requirements for land pattern on circuit boards

FOREWORD

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IEC 61188-6-1 has been prepared by IEC technical committee 91: Electronics assembly technology. It is an International Standard.

This first edition cancels and replaces the first edition of IEC 61188-5-1 published in 2002, and constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

a) The content is completely updated to reflect current industry requirements. See Introduction.

The text of this International Standard is based on the following documents:

Draft	Report on voting
91/1636/CDV	91/1671/RVC

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

A list of all parts in the IEC 61188 series, published under the general title *Circuit boards and circuit board assemblies – Design and use*, can be found on the IEC website.

Future documents in this series will carry the new general title as cited above. Titles of existing documents in this series will be updated at the time of the next edition.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

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INTRODUCTION

Explanation why the following standards will be replaced by the new IEC 6188-6 series:

IEC 61188-5-1:2002, *Printed boards and printed board assemblies – Design and use – Part 5-1: Attachment (land/joint) considerations – Generic requirements*

IEC 61188-5-2:2003, *Printed boards and printed board assemblies – Design and use – Part 5-2: Attachment (land/joint) considerations – Discrete components*

IEC 61188-5-3:2007, *Printed boards and printed board assemblies – Design and use – Part 5-3: Attachment (land/joint) considerations – Components with gull-wing leads on two sides*

IEC 61188-5-4:2007, *Printed boards and printed board assemblies – Design and use – Part 5-4: Attachment (land/joint) considerations – Components with J leads on two sides*

IEC 61188-5-5:2007, *Printed boards and printed board assemblies – Design and use – Part 5-5: Attachment (land/joint) considerations – Components with gull-wing leads on four sides*

IEC 61188-5-6:2003, *Printed boards and printed board assemblies – Design and use – Part 5-6: Attachment (land/joint) considerations – Chip carriers with J-leads on four sides*

IEC 61188-5-8:2007, *Printed board and printed board assemblies – Design and use – Part 5-8: Attachment (land/joint) considerations – Area array components (BGA, FBGA, CGA, LGA)*

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Content is mostly equivalent to IPC-782A with Amendments 1 and 2, which was replaced in 2002 by IPC-7351. The component spectrum and pitch levels have dramatically increased since publication of the IEC 61188-5 (all parts) and the dimensioning concept does no longer fulfil the mounting and soldering requirements.

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CIRCUIT BOARDS AND CIRCUIT BOARD ASSEMBLIES – DESIGN AND USE –

Part 6-1: Land pattern design – Generic requirements for land pattern on circuit boards

1 Scope

This part of IEC 61188 specifies the requirements for soldering surfaces on circuit boards. This includes lands and land pattern for surface mounted components and also solderable hole configurations for through-hole mounted components. These requirements are based on the solder joint requirements of the IEC 61191-1, IEC 61191-2, IEC 61191-3 and IEC 61191-4.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

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IEC 60194, *Printed board design, manufacture and assembly – Terms and definitions*

IEC 61191-1, *Printed board assemblies – Part 1: Generic specification – Requirements for soldered electrical and electronic assemblies using surface mount and related assembly technologies*

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IEC 61191-2:2017, *Printed board assemblies – Part 2: Sectional specification – Requirements for surface mount soldered assemblies*

IEC 61191-3, *Printed board assemblies – Part 3: Sectional specification – Requirements for through-hole mount soldered assemblies*

IEC 61191-4, *Printed board assemblies – Part 4: Sectional specification – Requirements for terminal soldered assemblies*

IEC 61760-3, *Surface mounting technology – Part 3: Standard method for the specification of components for through hole reflow (THR) soldering*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60194, and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1
assembly
number of parts, subassemblies or combinations thereof joined together

Note 1 to entry: This term can be used in conjunction with other terms listed herein, for example, "printed board assembly".

[SOURCE: IEC 60194:2015, 80.1327, modified – The second term "assembled board" has been removed.]

3.2
annular ring
portion of conductive material that completely surrounds a hole

3.3
basic dimension
numerical value used to describe the theoretical exact location of a feature or hole

Note 1 to entry: it is the basis from which permissible variations are established by tolerance on other dimensions in notes or by feature-control symbols.

[SOURCE: IEC 60194-1:2021, 3.2.24, modified – In the definition "for example a hole" has been replaced by "or hole".]

3.4
castellation
recessed metallised feature on the edge of a leadless chip carrier that is used to interconnect conducting surfaces or planes within or on the chip carrier

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[SOURCE: IEC 60194-1:2021, 3.3.17]

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3.5
component
individual part or combination of parts that, when together, perform (a) design function(s)

Note 1 to entry: See also "discrete component" in 3.4.17 of IEC 60194-2:2017.

[SOURCE: IEC 60194-2:2017, 3.3.19]

3.6
land
portion of a conductive pattern usually, but not exclusively, used for the connection and/or attachment of components

3.7
land pattern
footprint
combination of lands that is used for the mounting, interconnection and testing of a particular component

Note 1 to entry: Land pattern is also known as "footprint".

[SOURCE: IEC 60194-1:2021, 3.12.9]

3.8
nominal dimension
dimension that is between the maximum and minimum size of a feature (the tolerance on a nominal dimension gives the limits of variation of a feature size)

3.9
plated through-hole
PTH
hole with plating on its walls that makes an electrical connection between conductive patterns on internal layers, external layers, or both, of a printed board

[SOURCE: IEC 60194-1, 3.16.72, modified – The figure has been removed.]

3.10
printed board
PB
completely processed printed circuit and printed wiring configurations

Note 1 to entry: This includes single-sided, double-sided and multilayer boards with rigid, flexible, and rigid-flex base materials.

Note 2 to entry: "Printed board" is a general term.

[SOURCE: IEC 60194-2:2017, 3.16.23, modified – The second term "board" has been removed as well as the admitted terms "card" and "circuit card.]

3.11
registration
degree of conformity of the position of a pattern (or portion thereof), a hole, or other feature to its intended position on a product

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[SOURCE: IEC 60194-1:2021, 3.18.28]

3.12
soldering surface
solderable metallized surfaces on circuit boards

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Note 1 to entry: This includes lands, annular rings and solderable surfaces of plated through-holes.

3.13
SOIC
small outline integrated circuit
surface-mount technology
SMT
technology where electrical connection of components is made to the surface of a conductive pattern of a printed board and does not utilize component lead holes

3.14
terminal
connection element of an electronic component

3.15
through-hole technology
THT
assembly process for mounting component packages where leads are passed through supported (plated-through) or unsupported (bare) holes in an interconnection substrate

3.16
via
plated through-hole that is used as an interlayer connection, but in which there is no intention to insert a component lead or other reinforcing material

Note 1 to entry: See also "blind via" and "buried via" in 3.2.57 and 3.2.118 of IEC 60194-1:2021.

[SOURCE: IEC 60194-1:2021, 3.22.15]

4 Design requirements

4.1 General

Although soldering surfaces are dimensionally defined and since they are a part of the printed board circuitry geometry, they are subject to the producibility requirements and are influenced by tolerances associated with plating, etching, assembly or other conditions. The producibility aspects also pertain to the use of solder mask and legend printing and the registration required between the solder mask and the conductor patterns. The smaller the component dimensions, the more is producibility influenced by solder mask and silkscreen thickness. For circuit boards with component packages size 1005M (0402 imperial size) and smaller, legend printing should be avoided because it can have detrimental effects on solder paste printing.

This document assumes that the land pattern follows the principle that under nominal conditions, the overlap of the component termination and the corresponding soldering land will be complete.

The dimensions used for component descriptions shall be taken from standards developed by industrial and/or standards bodies. Designers should refer to these standards for additional or specific component package dimensions. When packages are not standardized, manufacturer datasheets are the foundation for dimensioning.

NOTE 1 For a comprehensive description of the given circuit board and for achieving the best possible solder joints to the devices assembled, the whole set of design elements includes, in addition to the land pattern definition:

- solder mask;
- copper foil thickness;
- plating thickness;
- solder paste stencil;
- clearance between adjacent components;
- clearance between bottom of component and PCB surface, if relevant;
- keep-out areas, if relevant;
- suitable rules for adhesive applications.

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All of these design elements are commonly defined for the mounting conditions. This standard is limited to defining requirements for land patterns and includes recommendations for clearances between adjacent components and for other design elements.

NOTE 2 Heat dissipation aspects have not been taken into account in this document.

Heavier components (greater mass per land) require larger lands or annular rings. In some cases, the lands shown in the standard may not be large enough; in these cases, consideration of additional measures like gluing can be necessary.

The preferred land form should be rectangular with rounded corners. The area of the smallest circumscribed rectangle shall be equal to that of one land with straight corners.

4.2 Product classification

The IEC standard on soldering requirements (see IEC 61191-1) recognizes that electrical and electronic assemblies are subject to classifications by intended end-item use. Three general end-product types have been established to reflect differences in producibility, functional performance requirements, and verification (inspection/test) frequency. It should be recognized that there may be overlaps of equipment between types.

The user of the assemblies is responsible for determining the performance type of the product. The purchase contract shall specify the product type required and indicate any exceptions or additional requirements to the parameters, where appropriate.

Products are divided into levels A, B and C according to IEC 61191-1.

– LEVEL A: General electronic products

  Includes consumer products, some computers and computer peripherals, and hardware suitable for applications where the major requirement is functionality of the completed assembly.

– LEVEL B: Dedicated service electronic products

  Includes communications equipment, sophisticated business machines, and instruments where high performance and extended life is required, and for which uninterrupted service is desired but not mandatory. Typically the end-use environment would not cause failures.

– LEVEL C: High-performance electronic products

  Includes all equipment where continued performance or performance-on-demand is mandatory. Equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment shall function when required, such as life support systems and other critical systems.

4.3 General surface mount land and land pattern requirements

The land pattern for components on circuit boards have to be dimensioned in such a way that, regardless of the type of termination, a sufficient wettable surface on the circuit board is provided to form a reliable solder joint during the soldering process, whatever the soldering technique. This applies to the same extent to surface mounted components as to through-hole components.

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4.4 Component packages and soldering process

The circuit designer selects electronic components that fulfill the electrical requirements of the end product. With the components, the circuit designer also selects the component package with the terminals that allow to connect the components to the circuit board. Depending on the type of terminal, the possible soldering process is also determined. For good manufacturability, it is very important that the circuit designer knows the relationship between component packages and the possible soldering methods.

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4.5 Soldering surface requirements

4.5.1 Main soldering techniques

Each soldering process has its own requirements for the soldering surfaces. The two main soldering techniques are reflow soldering and several types of wave soldering. The main differences between both methods is the available amount of solder and the possibility of components to move during reflow soldering.

Due to the process characteristics of both soldering techniques, different land dimensions are required to form reliable solder joints and accurate placement of components after soldering.

4.5.2 Reflow soldering

Reflow soldering is the main soldering technique for soldering of surface mounted components. First solder paste is deposited to solderable surfaces of the circuit board and after that the components are placed on the solder paste. See Figure 1.

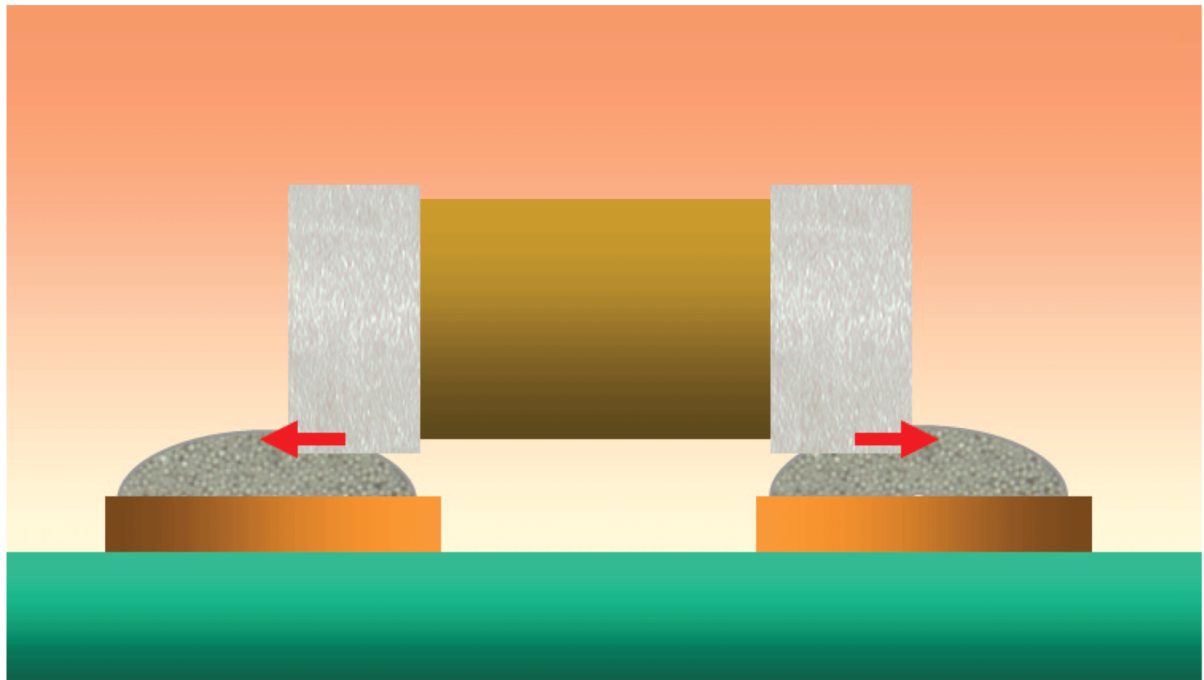

Figure 1 – Component placed on solder paste

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Typically, the components are only fixed by the stickiness of the flux. That is the reason why the components are swimming on the liquid solder during soldering and can be moved by the wetting forces of the solder.

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The dimensions of the soldering surfaces for reflow soldering on the circuit board are critical:

- if the land is too small, the amount of solder may be insufficient to form a reliable solder joint;
- if the land is too large, the wetting forces may move the component in one direction, which can cause displacement to the extent of an open solder joint occurring;
- if the land is too large and the wetting forces on the vertical side of the terminal are greater than on the bottom side, the component can be lifted by torque, leading to tombstoning and an open solder joint.
- if the finished land sizes on the circuit board are different for both terminals of the component, this imbalance also can cause tombstoning

4.5.3 Reflow soldering of leaded components

The process of reflow soldering of leaded components is called “through-hole reflow” or sometimes also “pin in paste”. In this process, special requirements shall be met with regard to the temperature resistance of components and the required volume of solder paste. The circuit board designer has to select components carefully depending on the type of solder paste used for reflow soldering. IEC 61760-3 shall be applied. Special care is required to apply enough solder paste to fill the hole around the component pins and form a reliable solder joint.

4.5.4 Wave soldering of surface mounted components

During wave soldering, the surface mounted components shall be fixed by glue because they are attached on the bottom surface of the circuit board. See Figure 2.

The board is then moved, face down, through the solder wave and the components are soldered.

There are only a limited number of surface mounted packages that can be wave soldered. The circuit board designer shall check the manufacturer datasheets concerning soldering process limitations.

For chip components smaller than 1608M (0603 imperial) and integrated circuits with pitches less than 1,27 mm (50 mil imperial) wave soldering is not recommended.

In contrast to reflow soldering, the available solder volume compared to the required solder volume to form a reliable solder joint is nearly unlimited. Additionally, as the components are glued and cannot move, there is no risk that the lands are too large.

To avoid solder bridges, components shall be placed at a safe distance from each other.

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IEC

Figure 2 – Component glued for wave soldering

Chip components should be placed parallel to the solder wave, integrated circuits like SO-packages with gullwing terminals should be placed parallel to the board transport direction and should be equipped with solder thieves. See Figure 3.