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TECHNICAL REPORT

colour inside

Process management for avionics – Electronic components capability in operation – Part 2: Semiconductor microcircuit lifetime

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PROCESS MANAGEMENT FOR AVIONICS – ELECTRONIC COMPONENTS CAPABILITY IN OPERATION –

Part 2: Semiconductor microcircuit lifetime

FOREWORD

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IEC TR 62240-2, which is a Technical Report, has been prepared by IEC technical committee 107: Process management for avionics.

IEC TR 62240-2 adapts and modifies the GIFAS/2015/5022 document that has served as a basis for the elaboration of this Technical Report.

The text of this Technical Report is based on the following documents:

Draft TR	Report on voting
107/325/DTR	107/332/RVDTR

Full information on the voting for the approval of this Technical Report can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

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INTRODUCTION

Electronic equipment for aerospace, defence and high performance (ADHP) applications integrate more and more commercial off the shelf (COTS) semiconductor microcircuits. These semiconductor microcircuits are above all designed and produced to address high volume and low cost markets such as consumer electronics, telecommunications or microcomputers, whose main requirements are basically cost, integration, performance and low consumption and for which the long term reliability in severe environments (for example vibration, thermal cycling, humidity and operating temperature) is not necessarily an imperative design criterion.

With semiconductor transistor feature size decrease, mainly from 90 nm transistor feature size, early wear-out can arise in COTS semiconductor microcircuits. For example, non-homothetic evolution of semiconductor microcircuit bias voltage and transistor feature size scaling have led to an increase of the electrical fields inside the semiconductor microcircuit and hence changes in classical failure and degradation modes or mechanisms. In addition new transistor architectures and technologies (for example fin field effect transistor (FinFET), fully depleted silicon on insulator (FD-SOI), etc.) and new materials (for example low-k dielectrics, high-k dielectrics, strain source/drain Si-Ge) have been introduced since the generation 90 nm to overcome the scaling issues, contributing potentially to the evolution of failure and degradation modes or mechanisms.

In this context, the lifetime of new generations of COTS semiconductor microcircuits may not meet the lifetime requirements of high performance, high reliability and long duration electronic applications (for example twenty years, thirty years or more). As a consequence, specific reliability assessment and maintenance plans are considered within the semiconductor microcircuit selection activities.

PROCESS MANAGEMENT FOR AVIONICS – ELECTRONIC COMPONENTS CAPABILITY IN OPERATION –

Part 2: Semiconductor microcircuit lifetime

1 Scope

This part of IEC 62240, which is a Technical Report, focuses on original equipment manufacturers (OEMs) using commercial off the shelf (COTS) semiconductor microcircuits for high performance, high reliability and long duration applications. This document supports OEMs in the preparation and maintenance of their semiconductor electronic component management plan (ECMP).

This document describes a process and a method for selecting digital semiconductor microcircuits by ensuring that their lifetime is compatible with the requirements of aerospace, defence and high performance (ADHP) applications (generally in connection with functional environments). Methods and guidelines are provided to assess the long term reliability of COTS semiconductor microcircuits in such applications; they mainly apply during the electronic design phase when selecting semiconductor microcircuits and assessing the application reliability.

Moreover, the document focuses on the intrinsic wear-out and the lifetime of COTS semiconductor microcircuits processed of less than or equal to 90 nm feature size (also called deep sub-micron (DSM) semiconductor microcircuits) and puts aside, at this time, packaging wear-out and random failure mechanisms. In this view, physics of failure (PoF) is at the heart of the approach.

NOTE 1 IEC 62239-1 can assist OEMs in the creation and maintenance of ECMPs.

NOTE 2 SAE ARP6338 can also help the OEM with regard to assessment and mitigation of early wear-out of life-limited semiconductor microcircuits.

NOTE 3 With the evolution of electronic technology and semiconductor microcircuits processed of less than or equal to 90 nm feature size, the current MIL-HDBK-217 handbook or FIDES guide become inappropriate as they are based for the time being on the assumption that the semiconductor electronic component exhibits a constant (random) failure rate and does not have life limits or exhibit wear-out.

Moreover, silicon itself has fundamentally very low failures in time (FIT) rates and the major failure modes are often in the packaging (for example housing, bond wires, etc.).

2 Normative references

There are no normative references in this document.

3 Terms, definitions and abbreviated terms

3.1 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1.1
acceleration model
equation for predicting time-to-fail as a function of operating stress

Note 1 to entry: An acceleration model shows how time-to-fail at a particular operating stress level can be used to predict the equivalent time-to-fail at a different operating stress level.

Note 2 to entry: An acceleration model is associated to one failure and degradation mode or mechanism. Acceleration models can be either defined for temperature, electrical, mechanical, environmental, or other stresses that can affect the reliability of a device.

Note 3 to entry: An acceleration model is semi-empirical and is basically based on the physics of failure. Times are generally derived from modeled time-to-failure distributions (lognormal, Weibull, exponential, etc.).

Note 4 to entry: The acceleration model is also defined as acceleration factor, for which the abbreviated term AF is used.

3.1.2
Bi-CMOS
bipolar CMOS
technology integrating two separate semiconductor technologies, bipolar junction transistor and CMOS transistor, in a single electronic component

3.1.3
cold redundancy
technique where one primary part is operational and the redundant one is in a backup mode

Note 1 to entry: The redundant part can also be called "cold" part and generally it is technically identical to the primary part.

Note 2 to entry: The "cold" part can be non-powered or in a standby mode and it is usually called upon only on failure of the primary part.

3.1.4
electronic equipment
functioning electronic device produced by the plan owner, which incorporates electronic components

Note 1 to entry: End items, sub-assemblies, line-replaceable units and shop-replaceable units are examples of electronic equipment.

[SOURCE: IEC 62239-1:2018, 3.20]

3.1.5
high-k dielectrics
material with a high dielectric constant "k" (as compared to silicon dioxide)

Note 1 to entry: High-k dielectrics are used in semiconductor manufacturing processes where they are usually used to replace a silicon dioxide gate dielectric or another dielectric layer of a semiconductor microcircuit. The implementation of high-k gate dielectrics is one of several strategies developed to allow continued scaling and miniaturization of semiconductor microcircuits.

3.1.6
lifetime
upper bound of period of time during which the COTS semiconductor component performs a required function without failure under stated conditions

3.1.7
low-k dielectrics
material with a small dielectric constant "k", relative to silicon dioxide

Note 1 to entry: Low-k dielectric material implementation is one of several strategies used to allow continued scaling and miniaturization of semiconductor microcircuits.

3.1.8
NAND
Negative-AND
logic gate which produces, in digital electronics, an output that is false (0) only if all its inputs are true (1) and an output true (1) if one or both inputs are false (0)

[SOURCE: IEC 62239-1:2018, 3.22]

3.1.9
NOR
Negative-OR
logic gate which produces, in digital electronics, an output that is true (1) if both the inputs are false (0) and an output false (0) if one or both inputs are true (1)

[SOURCE: IEC 62239-1:2018, 3.23]

3.1.10
plan owner
original design authority responsible for all aspects of the design, functionality and reliability of the delivered equipment in the intended application and responsible for writing and maintaining their specific ECMP

[SOURCE: IEC 62239-1:2018, 3.26]

3.1.11
process node
specific semiconductor manufacturing process and its design geometry rules

Note 1 to entry: Generally, a smaller technology node means a smaller feature size, producing smaller transistors which are both faster and more power-efficient. Historically, the name "process node" referred to a number of different features of a transistor including the gate length as well as the first layer metal half-pitch. Most recently, due to various marketing practices and discrepancies among foundries, the name "process node" has lost the exact meaning it once held. Recent technology nodes below 90 nm refer purely to a specific generation of semiconductor microcircuits made in a particular technology; they do not correspond to any gate length or half pitch. Nevertheless the name convention has stuck and it is what the leading foundries call their nodes.

Note 2 to entry: Process node is also called technology node or simply node.

3.1.12
semiconductor microcircuit
semiconductor electronic component
electrical or electronic device that is not subject to disassembly without destruction or impairment of design use and that utilises the properties of semiconductor materials

Note 1 to entry: It is sometimes called electronic part or electronic piece part or electronic device or electronic component or integrated circuits. It refers to active electronic parts such as memories, microcontrollers, microprocessors, etc.

3.1.13
wear-out
phenomenon resulting in a permanent physical degradation of a semiconductor that can be quantified through a quasi-deterministic lifetime indicator

3.2 Abbreviated terms

ADHP	aerospace, defence and high performance
AF	acceleration factor
BEOL	back end of the line
BTI	bias temperature instability
COTS	commercial off the shelf (related to semiconductor microcircuits for the purposes of this document)
CMOS	complementary metal-oxide semiconductor
DDR	double data rate (memory)
DPA	deprocessing analysis
DRAM	dynamic random access memory
DSM	deep sub-micron
ECMP	electronic component management plan
EM	electro-migration
EOT	equivalent oxide thickness
FD-SOI	fully depleted silicon on insulator
FEOL	front end of the line
FinFET	fin field effect transistor
FIT	failures in time (number of failures that can be expected in one billion device-hours of operation)
FPGA	field programmable gate array
Ge	germanium
HCI	hot carrier injection
I/O	input/output
MRAM	magnetic random access memory
NMOS	N metal-oxide semiconductor
OCM	original component manufacturer (related to the COTS electronic components manufacturer)
OEM	original equipment manufacturer
PMOS	P metal-oxide semiconductor
PoF	physics of failure
Si	silicon
SDRAM	synchronous dynamic random access memory
SRAM	static random access memory
TDDB	time dependent dielectric breakdown
$TTF_{X\%}$	time to failure (or lifetime) for x % of samples