

## IEC TR 61189-5-506

Edition 1.0 2019-06

# TECHNICAL REPORT



Test methods for **electrical materials**, printed boards, and other interconnection structures and assemblies – Part 5-506: General test methods for materials and assemblies – An intercomparison evaluation to implement the use of fine-pitch test structures for surface insulation resistance (SIR) testing of solder fluxes in accordance with IEC 61189-5-501 2c654b3a206a/iec-tr-61189-5-506-2019





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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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#### INTERNATIONAL ELECTROTECHNICAL COMMISSION

#### TEST METHODS FOR ELECTRICAL MATERIALS, PRINTED BOARDS AND OTHER INTERCONNECTION STRUCTURES AND ASSEMBLIES –

# Part 5-506: General test methods for materials and assemblies – An intercomparison evaluation to implement the use of fine-pitch test structures for surface insulation resistance (SIR) testing of solder fluxes in accordance with IEC 61189-5-501

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IEC/TR 61189-5-506, which is a technical report, has been prepared by IEC technical committee 91: Electronics assembly technology.

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The text of this Technical Report is based on the following documents:

Draft TR	Report on voting	
91/1500/DTR	91/1530A/RVDTR	

Full information on the voting for the approval of this Technical Report can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 61189 series, published under the general title *Test methods for electrical materials, printed boards and other interconnection structures and assemblies*, can be found on the IEC website.

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#### INTRODUCTION

This document addresses the development of IEC 61189-5-501 and the introduction of a finepitch test pattern. The introduction of this pattern is needed to meet the need for IEC 61189-5-501 to reflect current assembly technology. This document describes an intercomparison that tests a new test pattern and benchmarks it to existing test patterns. The work validates the introduction of the new fine-pitch test pattern.

It is well known that structures at fine pitches with flux residues are more susceptible to corrosion issues and electrochemical migration (ECM) problems. Characterization of flux residues in terms of ECM are commonly characterized using SIR testing. A key parameter of the SIR test is the comb pattern used and gap between the electrodes. The current B24 and B25 with their 500- $\mu$ m and 318- $\mu$ m gap patterns are not representative of fine pitches. It has been proposed to use a 200- $\mu$ m gap pattern, and this document describes an intercomparison that validates the introduction of the 200- $\mu$ m gap pattern.

This document describes an exercise that used a new test board that included the B24 and B25 patterns with an additional 200-µm pattern, with each pattern duplicated, giving six patterns in all on each test board. This work was motivated by an update to IEC 61189-5-501. A protocol for the testing was developed that took a standardised test rosin flux and defined the flux loading and thermal conditioning. Seven laboratories took part from five countries. The test boards were prepared centrally and then tested in the seven laboratories, and the results analysed to validate the usage of the 200-µm pattern. The document describes the intercomparison and the data analysis.

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Part 5-506: General test methods for materials and assemblies – An intercomparison evaluation to implement the use of fine-pitch test structures for surface insulation resistance (SIR) testing of solder fluxes in accordance with IEC 61189-5-501

#### 1 Scope

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This Technical Report is an intercomparison supporting the development of IEC 61189-5-501 in relation to the SIR method. This document sets out to validate the introduction of a new 200- $\mu$ m gap SIR pattern, and was benched marked against existing SIR gap patterns of 318  $\mu$ m and 500  $\mu$ m.

#### 2 Normative references

There are no normative references in this document.

#### iTeh STANDARD PREVIEW Terms and definitions

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No terms and definitions are listed in this document.

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#### 4 Test board concept for intercomparison

#### 4.1 The need for a fine-pitch SIR pattern

The pursuit of higher quality and reliability leads to the requirement of proving that electronic assemblies are not susceptible to electrochemical failure. Such robustness will lead to proven lifetime performance in the field. Electrochemical failure can occur at the surface or subsurface, and in this paper we focus on surface failure phenomena and its characterisation. Electrochemical failure needs three factors to be present simultaneously for a failure to occur: a continuous water film, an applied electric filed, and soluble ionic material. Under condensing conditions, a macroscopic water film will form and in most instances an uncoated assembly will fail instantly. But for high humidity conditions, an invisible sub-micron water film will form that will support low levels of conduction, and certainly no fast dramatic loss of isolation. Applied electric fields can cause electrochemical failure, from 25V/mm and upwards, by driving ions down an electric field. Ionic material is needed as pure water has very high resistivity, hence dissolved ions increase conductivity and polarization at electrodes resulting in corrosion at anodes. Sources of contamination can appear on the surface of the assembly from the manufacturing process or the environment. If the contamination is water soluble and dissociates to form ionic species, these ions migrate under an electric field.

It is of course of interest as to what ionic materials are present, but more importantly, the question is what will be the impact of these residues or contamination. The industry many years ago developed the basis of the "Surface Insulation Resistance" test, which applies an

electrical bias across an interdigitated comb in a damp heat environment at elevated temperatures and measures the resistance stability. This test is a simulation of what will happen in the field, and hence the outcome is relevant to that performance. The IPC TM650 2.6.3.3, 2.6.3.6 and 2.6.3.7 describe the SIR test for various applications, providing various test geometries and voltage conditions. The B24 has a 500-µm gap in the comb pattern, and this is typically a lot greater than the minimum distances found on high-density circuit assemblies, where the gap can easily be down to 200 µm and below. The B24 was proposed circa 1990 and reflected the needs of those days, and of course since then there has been a move to finer pitches. At finer gaps, the electrochemical behaviour can accelerate and is sensitive to the applied electric field (see NPL work from 2000). In this work, it was shown for certain residues that as the test voltage dropped, so did the measured resistance, hence the electrochemical pathway did not behave in a simple ohmic manner. A conclusion of this work was that the gap in the SIR pattern and the applied voltage should be representative of the intended use environment. Hence, within IPC 2.6.3.7 there is a recommendation to use a 200µm pattern with a 25V/mm field strength. No SIR pattern is given there. However, within the IPC-B-52 there are 200-µm SIR patterns used, specifically below the QFP devices.

Therefore, there is a strong interest in using the 200- $\mu$ m SIR pattern but there is not a dedicated test coupon available. This paper sets out to demonstrate the interoperability of using different SIR patterns and hence demonstrate that the 200- $\mu$ m pattern can be used with confidence. Most SIR patterns are approximately 25 mm × 25 mm, and as the pitch of the interdigitated comb decreases, the so-called number of squares increases. As the number of squares increases, the resistance will drop. Hence, if we consider the case where there is a fixed resistance for any square, as the number of squares increases, the overall measured resistance of the pattern will decrease, since these squares are in parallel. Any comparison shall therefore take into account the number of squares in the SIR pattern.

The electrochemical behaviour in the SIR test is known to be pitch-sensitive, and as the pitch reduces, the incidence of dendrites increases, even when the field strength is held constant. The potential for this catastrophic failure is the motivation for this intercomparison, but it is not something we wish to soccur here/cRathen, we are rattempting to demonstrate that under intermediate SIR values ( $10^8 \Omega$  and above), the patterns behave in an identical way, allowing for differences in the number of squares. Hence a test regime will be invoked that causes this behaviour and allows a straightforward comparison between the various pitches in this study.

In this study, we have taken a 200- $\mu$ m gap pattern in common use, and originally defined in a joint European project. This pattern will be compared with two SIR patterns in common use today, the IPC B24 and a pattern from the B25, with 400  $\mu$ m/500  $\mu$ m and 318  $\mu$ m/318  $\mu$ m track and gap, respectively. A board was designed that included these three SIR patterns, duplicating each pattern, and named TB144.

To validate the introduction of this new test-pattern, an intercomparison exercise was undertaken, with seven laboratories taking part, from Denmark, Germany, Japan, the UK, and the USA. The laboratories were: Alpha Assembly Solutions, Gen 3 Systems, Hytek, National Physical Laboratory (NPL), Nihon Genma MFG. CO. Ltd, Robert Bosch GmbH Automotive Electronics, and Rockwell Collins<sup>1</sup>.

#### 4.2 Test board design

This round robin sets out to establish the justification for using a finer-pitch pattern. The test PCB has three SIR pitch patterns, two current designs (IPC B24 and a pattern from the B25, with 400  $\mu$ m/500  $\mu$ m and 318  $\mu$ m/318  $\mu$ m track and gap, respectively), and a finer-pitch pattern with a 400  $\mu$ m/200  $\mu$ m track and gap pattern. A board was designed and this board currently has the name TB144, and is shown below.

<sup>1</sup> This information is given for the convenience of the users of this document and does not constitute an endorsement by IEC of the laboratories named.

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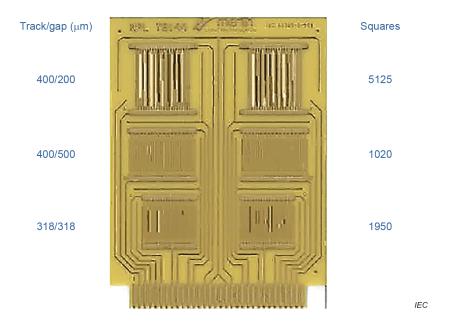


Figure 1 – TB144

In Figure 1, the number of squares is also given, and as can be seen, the number of squares for the 400  $\mu$ m/200  $\mu$ m pattern are significantly higher. It can also be seen that there are only small differences in overall size between the patterns. All test patterns have the same applied voltage and, in this work, was set to 20 V. This meant that the electric field strength was different for the three SIR patterns, as occurs on products. The impact of these changes are shown in Table 1. The intercomparison will establish the relative performance of the new pattern, prior to its inclusion in a new standard 9-5-506:2019

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Table413+2SIR pattern9nformation						

	B24	B25	New
Track/Gap (μm)	400/500	318/318	400/200
Number of squares	1 020	1 950	5 125
Resistance (Ω) <sup>a</sup>	1,00E+08	5,23+07	1,99+07
Field Strength (V/mm) <sup>b</sup>	40,0	62,9	100,0

<sup>a</sup> The  $10^8 \Omega$  is an example value for the pattern and the two following values assume the same resistance per square, and calculated the drop in resistance caused by the increase in the number of squares.

<sup>b</sup> The field strength is calculated using an applied bias of 20 V.

#### 4.3 Test board fluxing

All six patterns were dosed with the same density of an activated rosin flux and tested under two climatic conditions, 40  $^{\circ}$ C/93  $^{\circ}$  RH, and 85  $^{\circ}$ C/85  $^{\circ}$  RH. All test boards were cleaned and then fluxed at NPL by a single operator and shipped to the test house 2 weeks before commencement of the testing.

Each test house, after completing the analysis and inspection, returned the data to the coordinator, NPL, for analysis.

- The project provided test boards, sourced from a single PCB fabricator. The PCBs were made from 152 g/m<sup>2</sup> (0,5 oz/ft<sup>2</sup>) Cu and EM-827 high Tg laminate.
- 2) The flux used is given in Table 2.