IEC TR 62878-2-7

Edition 1.0 2019-03

TECHNICAL REPORT

colour inside

Device embedding assembly technology
Part 2-7: Guidelines – Accelerated stress testing of passive embedded circuit boards

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DEVICE EMBEDDING ASSEMBLY TECHNOLOGY

Part 2-7: Guidelines – Accelerated stress testing of passive embedded circuit boards

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IEC TR 62878-2-7, which is a technical report, has been prepared by IEC technical committee 91: Electronics assembly technology.

The text of this technical report is based on the following documents:

Enquiry draft	Report on voting
91/1553/DTR	91/1559/RVDTR

Full information on the voting for the approval of this technical report can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 62878 series, published under the general title *Device embedding assembly technology*, can be found on the IEC website.

Future standards in this series will carry the new general title as cited above. Titles of existing standards in this series will be updated at the time of the next edition.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

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- replaced by a revised edition, or
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DEVICE EMBEDDING ASSEMBLY TECHNOLOGY

Part 2-7: Guidelines – Accelerated stress testing of passive embedded circuit boards

1 Scope

This part of IEC 62878 describes the accelerated stress testing of passive embedded circuit boards. It can be used for screening finished boards, including multilayer and high-density interconnection (HDI) boards. These boards are mainly for mobile devices.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60194, *Printed board design, manufacture and assembly - Terms and definitions*

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3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60194 apply.

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ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

4 Overview of accelerated stress testing of passive embedded circuit boards

4.1 Testing under combined stresses

A combined test method has been used to simulate real world conditions. It is a combination of a thermal stress by heating at high temperature, an environmental stress at 85 °C/ 85 % RH, and a mechanical stress with vibration. In order to test specimens under various stresses, a bending tester with heat generating specimens was put into the thermo-hydrostat. The reliability can be checked by monitoring output voltage of the heated sample as shown in Figure 1. The heating temperature is set to 325 °C in order to shorten the testing time to 1 h for boards fabricated with a high temperature of decomposition (T_d) material (T_d > 350 °C). The testing can be done at 305 °C for 1,5 h if material with a lower T_d is used.

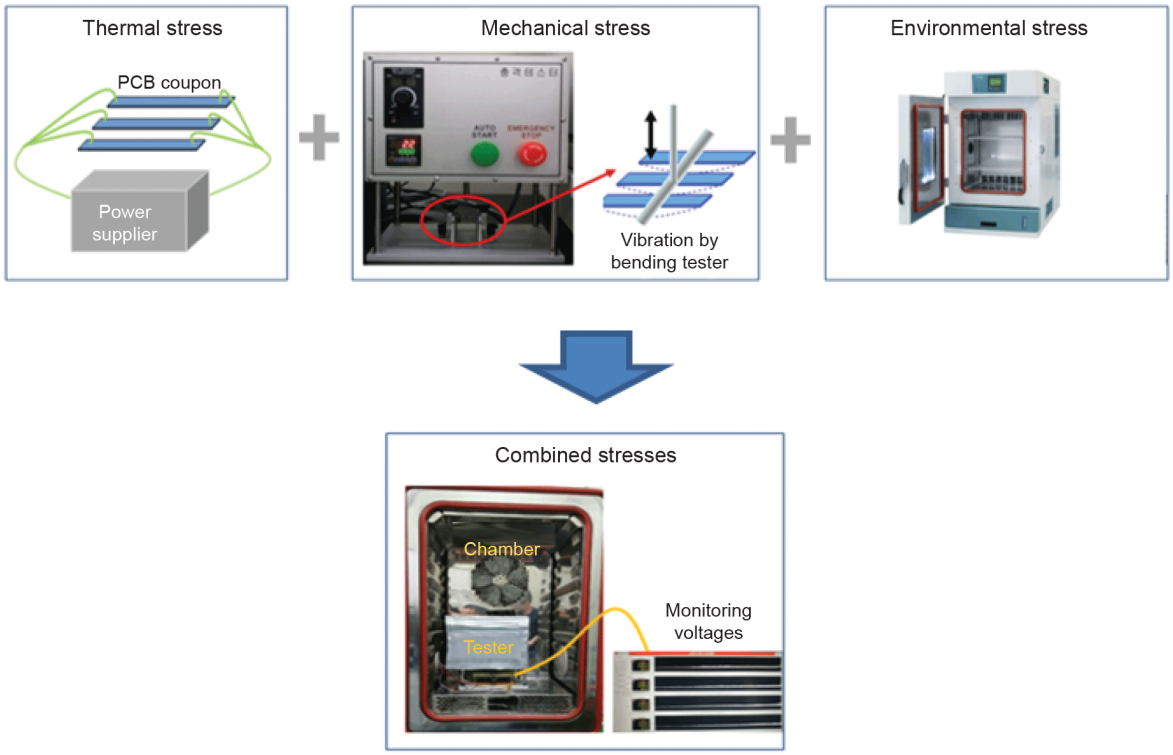

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Figure 1 – Testing principal

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4.2 Test coupon design

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Four test coupons are built in a test area of passive embedded circuit board panel as shown in Figure 2. Each test coupon has circuits connecting embedded passives, as shown in Figure 3, that act as heating circuits as well. They are fabricated in accordance with the design rules in Annex A. The design and layer specifications are shown in Tables 1 and 2. The circuits of the top and the bottom layers are the same.

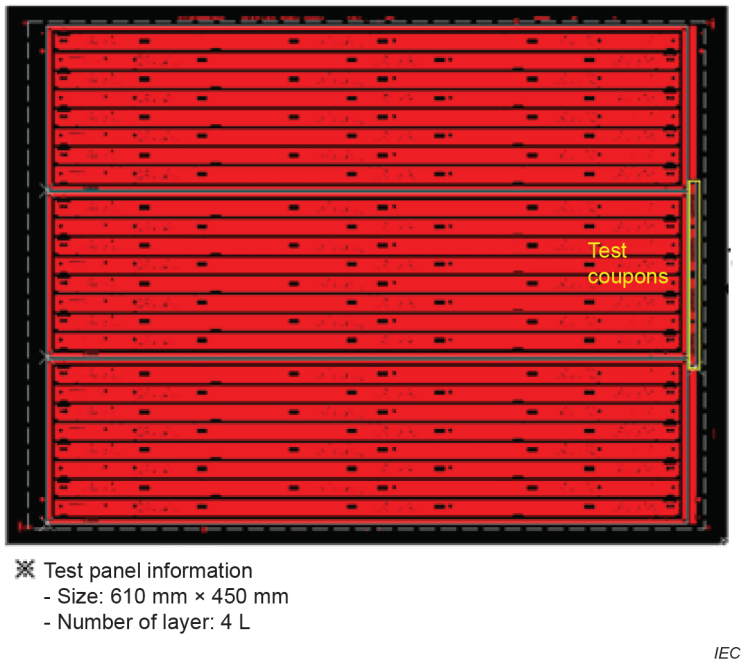

Figure 2 – Embedded circuit board panel with test coupons

Table 1 – Design information for test coupon

Line width	100 µm
Via pad	350 µm
Distance between embedded components	450
Ground connection size	7,28 mm × 2 mm
Coupon size	35 mm × 5 mm

Table 2 – Stack-up information for test coupon

Layer	Thickness (µm)
Solder resistor	20
Circuits (copper)	30
Dielectric (prepreg)	60
Circuits (copper)	35
Dielectric (FR4 core)	250
Circuits (copper)	35
Dielectric (prepreg)	60
Circuits (copper)	30
Solder resistor	20
Total	540 ± 54

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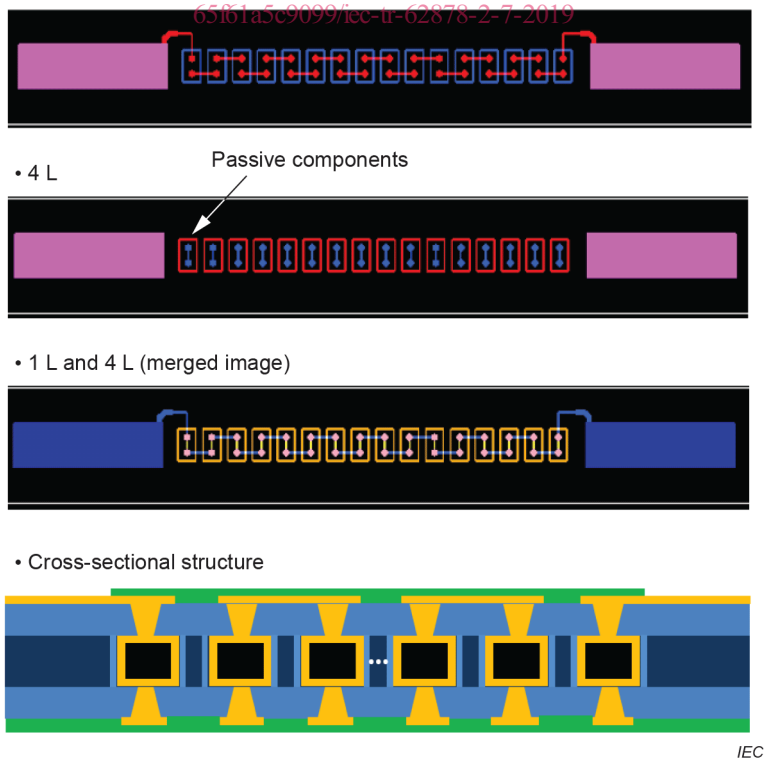

Figure 3 – Test coupon structure