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INTERNATIONAL STANDARD

colour inside

Printed electronics – Part 503-3: Quality assessment – Measuring method of contact resistance for the printed thin film transistor – Transfer length method

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PRINTED ELECTRONICS –

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FOREWORD

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International Standard IEC 62899-503-3 has been prepared by IEC technical committee 119: Printed Electronics.

The text of this International Standard is based on the following documents:

FDIS	Report on voting
119/359/FDIS	119/368/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

A list of all parts in the IEC 62899 series, published under the general title *Printed electronics*, can be found on the IEC website.

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- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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INTRODUCTION

In a thin film transistor (TFT), contact resistance occurs at the contacting interfaces at the gate, source and drain electrodes, and the TFT semiconductor layer. While contact resistance is negligible at the gate electrode, it reduces the effective voltage applied to the source and drain electrodes. Therefore, the evaluation of the contact resistance can provide important insights related to the performance characteristics of printed TFTs. Especially for printed electronics, the contact resistance varies with the employed materials, printing processes and the time series variation because the interface is made of simple contact obtained by additive manufacturing instead of a junction obtained by vacuum deposition and etching processes. Thus, the performance of printed TFTs is greatly influenced by the value of contact resistance. A change of the contact resistance is therefore considered to be a key factor for a proper interpretation of performance, lifetime, and reliability of a printed TFT.

To determine the contact resistance, several techniques, including but not limited to two-terminal contact method, four-terminal contact method, six-terminal contact method, transfer length method, and scanning probe potentiometer technique can be used. The transfer length method (TLM) in particular has a practical advantage because the supplier can test discrete devices, which have the same structure as the original printed TFT, on a common substrate simultaneously. Furthermore, the TLM is cost-effective because the user can measure the apparent contact resistance without using expensive equipment. Therefore, by using TLM, the supplier and the user can exchange the important parameter of the TFT that is contact resistance for reliability assessment as a part of their supply chain service.

PRINTED ELECTRONICS –

Part 503-3: Quality assessment – Measuring method of contact resistance for the printed thin film transistor – Transfer length method

1 Scope

This part of IEC 62899 specifies a measuring method of contact resistance for printed thin film transistors (TFTs) by the transfer length method (TLM). The method requires the fabrication of a test element group (TEG) with varying channel length (L) between source and drain electrodes. The method is intended for quality assessment of TFT electrode contacts and is suited for determining whether the contact resistance lies within a desired range.

2 Normative references

There are no normative references in this document.

3 Terms and definitions

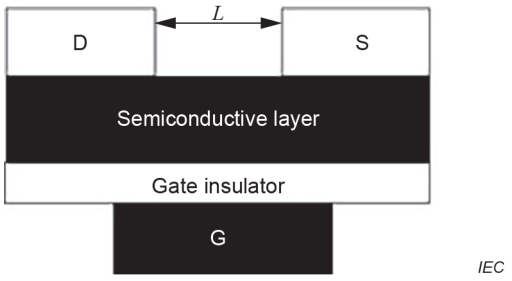
For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

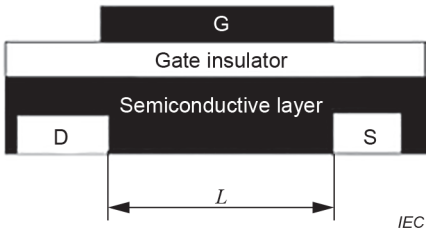
- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1
contact resistance
R_C
<printed thin film transistor> resistance at the interface between an electrode and the semiconductor layer in a printed thin film transistor

Note 1 to entry: The resistance of the interface in this document involves not only the contacting area between the electrode and the semiconductor layer but also the semiconductor layer between the contacting area to electrode and the channel area for the "bottom-gate and top-contact" and "top-gate and bottom contact" devices shown in Figure 1, respectively.



(a) 'bottom-gate and top-contact' device



(b) 'top-gate and bottom contact' devices

Key

S source electrode

D drain electrode

G gate electrode

L distance between source and drain electrodes, i.e. channel length

Figure 1 – Schematic structure of printed thin film transistors (TFTs)

3.2
drain voltage
V_d
voltage which is applied between the drain electrode and source terminal (ground) of the transistor

3.3
gate voltage
V_g

voltage which is applied between the gate electrode and source terminal (ground) of the transistor

3.4
transfer length method
TLM
method to determine R_c by the preparation of sets of thin film transistors and measurements of resistances for each transistor with their variation of distances between source and drain, i.e. channel length L

Note 1 to entry: This method is applied in the linear regime of the TFT, which is defined as $|V_d|<|V_g|-|V_t|;|V_g|>|V_t|$.

3.5
pinch-off voltage
voltage at which $|V_d|=|V_g|-|V_t|;|V_g|>|V_t|$

4 Symbols and abbreviated terms

For the purposes of this document, the following symbols and abbreviated terms apply.

R_c contact resistance

TFT thin film transistor

TEG test element group (TFT device prepared for estimation of R_c)

TLM transfer length method

V_d drain voltage

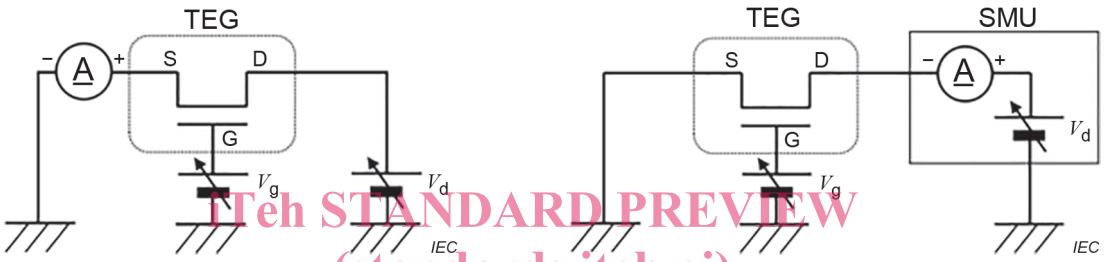
V_g gate voltage

V_t threshhold voltage

5 Measuring method of contact resistance

5.1 General

Total resistance from the source to the drain consists of two resistances, namely, the semiconductor channel resistance and the source and drain contacts' resistance. In the TLM method, the contact resistance is expressed by extrapolation of the total resistance for TFTs with different source-drain channel lengths L to $L = 0$, which eliminates the semiconductor channel resistance and yields the contacts' resistance as the y-intercept. The schematic diagram for the measurement of the contact resistance is shown in Figure 2. Clause 5 specifies the preparation of the TEGs, the measuring apparatus, the measuring procedure and the reporting items. Individual measuring conditions and reporting items may be decided by agreement between supplier and customer.



(a) using current meter **(b) using SMU (source measurement unit)**

Key

S source electrode

D drain electrode

G gate electrode

Figure 2 – Measurement configuration

5.2 Preparation of TEGs

The supplier of the printed TFTs prepares the TEGs for the measurement of the contact resistance of printed TFTs which have been used in the manufacture of electronic assemblies or circuits.

TEGs shall be fabricated using the same materials and device architecture as the TFTs to be characterised and shall be prepared on the same substrate. TEGs might be prepared on a different substrate when it is extremely difficult for the supplier to produce such TEGs or for the user to measure their electronic properties.

The cross-sectional structure of a TEG which includes materials, thickness, deposition processes of each device components such as source electrode, drain electrode, gate electrode, semiconductor, insulator, encapsulation/protection, and other transistor elements shall be the same as used in the evaluated TFT.

The semiconductor shall cover the whole channel area (made of width W and length L). The gate electrode shall cover the whole channel area.

A set of TEGs shall include four or more TEGs which have different distances (i.e. channel lengths L) between source and drain electrodes, as shown in Figure A.1 (see Annex A).