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INTERNATIONAL STANDARD

NORME INTERNATIONALE

Semiconductor devices – Reliability test method by inductive load switching for gallium nitride transistors

Dispositifs à semiconducteurs – Méthode d'essai de fiabilité par la commutation sur charge inductive pour les transistors au nitrure de gallium

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SEMICONDUCTOR DEVICES – RELIABILITY TEST METHOD BY INDUCTIVE LOAD SWITCHING FOR GALLIUM NITRIDE TRANSISTORS

FOREWORD

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Draft	Report on voting
47/2753/FDIS	47/2763/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

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- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

INTRODUCTION

Gallium nitride (GaN), one of the wide bandgap semiconductors, has superior properties over conventional silicon (Si) for power devices, such as high breakdown electric field and high saturation velocity. Two dimensional electron gas with high mobility and high concentration is induced by forming heterojunction of GaN with aluminum gallium nitride (AlGaN) due to polarization effects, which is another merit of GaN related materials. Moreover, several kinds of materials such as Si, sapphire, silicon-carbide (SiC) or GaN can be selected as epitaxial growth substrates in terms of device performances and costs. Recently, GaN power transistors have been widely developed and commercialized.

GaN power transistors have some unique failure modes due to device construction differences and carrier trapping effects. In addition, GaN power transistors are more compact, so are exposed to higher fields. Further, some hot-carrier and robustness tests for silicon Field Effect Transistors (FETs) are not applicable to GaN FETs. For example, the hot carrier injection (HCI) test for lateral MOSFETs is not applicable to lateral GaN FETs due to the blocking nature of the buffer, and the unclamped inductive switching (UIS) test is not useful because it could cause damage. Therefore, several unique reliability test methods, which are not generally requested for Si power transistors, are performed as reliability examination, for example, test methods of dynamic on-resistances. Especially, switching test methods and reliability procedures are significant for practical use and need to be standardized in order to establish switching reliability of GaN power transistors.

This document is a guideline focusing on inductive load switching in order to confirm the conditions under which GaN power transistors are used reliably. Since the inductive load switching is considered to be an important stress application for power devices, this guideline will promote the acceptance of GaN power transistors in the power device market. However, it is important to note that there are other application-relevant stress conditions, such as soft-switching at high frequencies, which will not be covered by this document.

SEMICONDUCTOR DEVICES – RELIABILITY TEST METHOD BY INDUCTIVE LOAD SWITCHING FOR GALLIUM NITRIDE TRANSISTORS

1 Scope

This document covers the protocol of performing a stress procedure and a corresponding test method to evaluate the reliability of gallium nitride (GaN) power transistors by inductive load switching, specifically hard-switching stress.

2 Normative references

There are no normative references in this document.

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
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3.1
gallium nitride
GaN
compound semiconductor material composed of gallium and nitrogen

3.2
aluminum gallium nitride
AlGaN
compound semiconductor alloy of aluminum nitride and gallium nitride

3.3
on-state resistance
resistance of the device at nominal current conditions

3.4
dynamic on-state resistance
ratio of on-state drain-source voltage(v_{DS}) to drain current(i_{D}) at switching

3.5
dynamic high temperature operating life test
DHTOL test
reliability test of continuous switching stress with high junction temperature

Note 1 to entry: The term DHTOL is used broadly, encompassing both switching accelerated life test (SALT), where failures are expected for wearout modelling, and HTOL, where failures are not expected.

3.6
switching locus
trajectory showing relationship between v_{DS} and i_{D} during switching

4 Objectives

The purpose of this document is to define a reliability test method for finding conditions under which GaN power transistors can operate reliably, when they are used for continuous hard switching with inductive loads. Therefore, this document does not cover other application-relevant stress conditions, such as third quadrant operation and soft-switching or other types of circuit topologies.

5 Applicable GaN transistors

This test method can be applied to all power transistors, which include GaN power transistors with any substrate such as Si, SiC, sapphire or GaN, and to lateral or vertical types. Moreover, this test method can be applied to any gate structure such as Schottky-types, p-type GaN (p-GaN) types and MIS (metal-insulator-semiconductor) types. It can also be applicable to normally-off types, normally-on types and to cascode configuration types.

6 Dynamic high temperature operating life test

6.1 Test sample

The test sample is recommended to be an actual packaged product. For family products, reliability test results of transistors with large gate widths can be applied to transistors with small gate widths when use conditions such as current density and supply voltage are equivalent or less.

6.2 Test circuit

6.2.1 Scheme of a hard switching circuit

The dynamic high temperature operating life (DHTOL) test employs a hard switching circuit with an inductive load as shown in Figure 1.

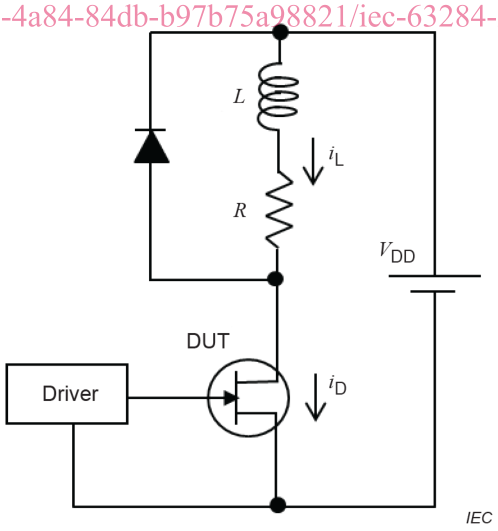

Figure 1 – Test circuit

6.2.2 Electrical parameters

Frequency f, power supply voltage V_{DD}, and average current flowing through inductance $I_{L(AV)}$ are set by considering the actual operating condition.

6.2.3 Diode

A diode is selected by considering the maximum current and the maximum voltage. In particular, since the recovery current of the diode flows to the transistor at turn-on time, the diode is selected to replicate the switching conditions of the final application, e.g. emulate the capacitance of the high-side FET, or have a larger capacitance for accelerated stress.

6.2.4 Gate driver

A test circuit including a gate drive circuit suitable for the individual test transistor is constructed with attention paid to heat dissipation of each component. The gate driver is required to drive DUT in the same conditions as the actual usage unless switching parameters to acquire acceleration factors are included. Note that the gate driver is also required to have current driving capability so as not to cause false turn-on of the DUT.

6.2.5 Inductance and resistance

An inductance value L_C and a resistance value R_L are set with reference to the following Equation (1) to Equation (3) and the switching waveforms in Figure 2.

$$L_\text{C} \times \frac{\Delta I}{t_1} = V_\text{DD} - I_\text{L(AV)} \times R_\text{L} \tag{1}$$

$$L_\text{C} \times \frac{\Delta I}{t_2} = I_\text{L(AV)} \times R_\text{L} + V_\text{F} \tag{2}$$

$$f = \frac{1}{t_1 + t_2} \tag{3}$$

where

V_DD	is the power supply voltage;
$I_\text{L (AV)}$	is the average current;
ΔI	is the ripple current;
V_F	is the threshold voltage of diode;
L_C	is the coil inductance value;
R_L	is the load resistance value;
t_1	is the on time;
t_2	is the off time;
f	is the switching frequency.

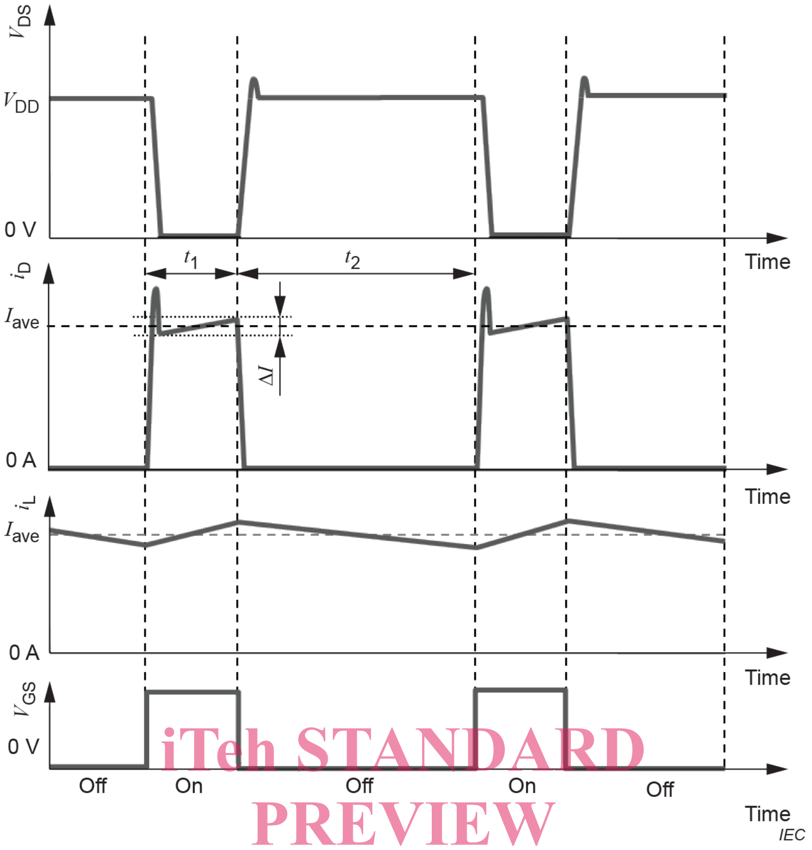

Figure 2 – Wave forms of switching

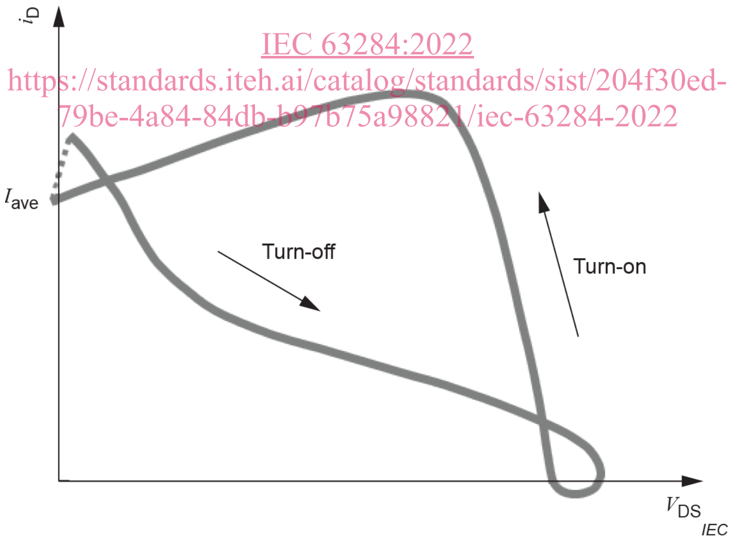

Figure 3 – Switching locus at hard switching

6.3 Test condition

6.3.1 General

After the test circuit is configured, electrical and thermal stress conditions are applied and evaluated.

6.3.2 Electrical stress

A switching locus of the test transistor is constructed by using switching wave forms as shown in Figure 3. It is confirmed that the current and voltage stress conditions are equivalent to or greater than the actual application. For more details on how to assess whether the current and voltage stress is equivalent to the actual application, refer to JEDEC JEP180.01, Clause 5 [1][1].

6.3.3 Thermal stress

External heating and/or cooling may be used in order that thermal stress is independently varied without changing other stress conditions. When other stress conditions are varied with minimizing effects of variation in junction temperature, the relative changes of the junction temperature should be monitored by a thermocouple provided as close as possible to the DUT or by a thermo-viewer. The junction temperature is recommended to be equal to or below the absolute maximum rating temperature. The protocol is described in 6.6 if a more accelerated temperature is used.

6.4 Test procedure

6.4.1 Flow chart

A flow chart of the DHTOL test is shown in Figure 4. In the flow chart, the procedure is aimed at accelerated life testing (ALT).

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[1] Numbers in square brackets refer to the Bibliography.