IEC 63275-1

Edition 1.0 2022-04

INTERNATIONAL STANDARD

NORME INTERNATIONALE

**Semiconductor devices – Reliability test method for silicon carbide discrete metal-oxide semiconductor field effect transistors –
Part 1: Test method for bias temperature instability**

**Dispositifs à semiconducteurs – Méthode d'essai de fiabilité pour les transistors à effet de champ métal-oxyde-semiconducteurs discrets en carbure de silicium –
Partie 1: Méthode d'essai pour la mesure de la dérive de la tension de seuil après polarisation électrique en température**

IEC 63275-1:2022-04(en-fr)

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INTERNATIONALE

ICS 31.080.30

ISBN 978-2-8322-1101-5

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**SEMICONDUCTOR DEVICES –
RELIABILITY TEST METHOD FOR SILICON CARBIDE DISCRETE
METAL-OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTORS –**

Part 1: Test method for bias temperature instability

FOREWORD

IEC 63275-1 has been prepared by IEC technical committee 47: Semiconductor devices. It is an International Standard.

The text of this International Standard is based on the following documents:

Draft	Report on voting
47/2755/FDIS	47/2764/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

A list of all parts in the IEC 63275 series, published under the general title *Semiconductor devices – Reliability test method for silicon carbide discrete metal-oxide semiconductor field effect transistors*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

INTRODUCTION

One reliability issue for silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) is gate-source threshold voltage shift under gate-source voltage stress. Gate-source threshold voltage is a key parameter to represent switching characteristics of MOSFETs. Since the shift value tends to be larger than that of conventional Si based devices, it is indispensable to establish an International Standard with regard to evaluation of gate-source threshold voltage shift as a reliability issue.

This document defines the evaluation method of gate-source threshold voltage shift under continuous temperature and gate-source voltage stress on SiC MOSFETs.

**SEMICONDUCTOR DEVICES –
RELIABILITY TEST METHOD FOR SILICON CARBIDE DISCRETE
METAL-OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTORS –**

Part 1: Test method for bias temperature instability

1 Scope

This part of IEC 63275 gives a test method to evaluate gate threshold voltage shift of silicon carbide (SiC) power metal-oxide-semiconductor field-effect transistors (MOSFETs) using room temperature readout after applying continuous positive gate-source voltage stress at elevated temperature. The proposed method accepts a certain amount of recovery by allowing large delay times between stress and measurement (up to 10 h).

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60747-8, *Semiconductor devices – Discrete devices – Part 8: Field-effect transistors*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60747-8 apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

4 Requirements

4.1 Sample

Unless otherwise specified, a minimum of four samples is recommended for each test condition to evaluate representative behaviour of $V_{GS(th)}$ drift. When the test method is applied to qualify reliability of product, the sample size should be defined by taking into consideration device-to-device deviation of shift value of $V_{GS(th)}$ and target application of the product.

4.2 Test temperature

The test is performed at the temperature within the maximum rating of the sample.

4.3 Test voltage

The test is performed at the V_{GS} within the maximum rating of the sample. The tests in this document treat only positive V_{GS} stress.

4.4 Test time

Test time is set individually to reach failure criteria of $V_{GS(th)}$ or to collect data required to extrapolate the log time dependence to reach failure criteria $V_{GS(th)}$. The time for temperature ramping and measuring $V_{GS(th)}$ shall not be added to the stress time.

4.5 Measurement temperature

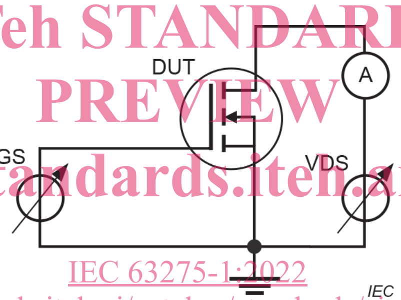
Measurement is performed at room temperature with a tolerance, e.g. 23 °C ± 2 °C. The measurement temperature shall be consistent across the evaluation.

4.6 Failure criteria

It is recommended to link the failure criteria to a maximum allowed $V_{GS(th)}$ drift level that does not cause the violation of any data sheet specification limit.

4.7 Test circuit

Figure 1 shows the test circuit. VGS, voltage source for the V_{GS} is the voltage source to apply V_{GS} on a sample. VDS, voltage source for the V_{DS} is the voltage source to apply V_{DS} on a sample for $V_{GS(th)}$ measurement.



Key

A	ammeter to measure drain source current of DUT
DUT	device under test sample
VGS	voltage source for the V_{GS}
VDS	voltage source for the V_{DS}

Figure 1 – Circuit diagram for bias temperature instability test

5 Procedures

5.1 Sequence of procedure

The test method evaluates the shift value of $V_{GS(th)}$ by alternately conducting $V_{GS(th)}$ measurement and applying temperature and voltage stress on the gate terminal of the sample. Figure 2 shows the test flow chart.

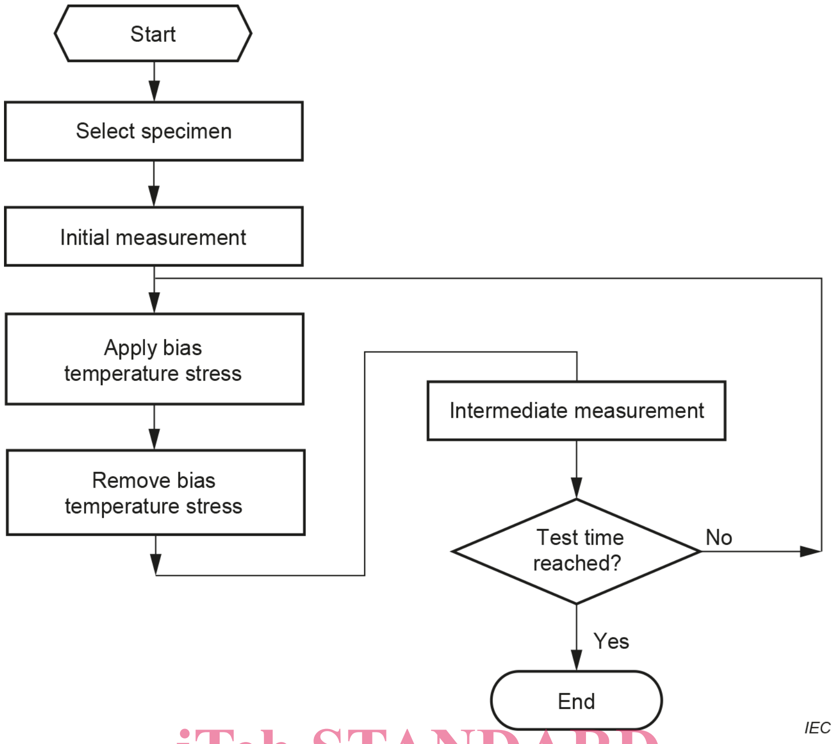


Figure 2 – Test flow chart

5.2 Select sample

Select and set the sample to the test apparatus.

5.3 $V_{GS(th)}$ measurement methods

$V_{GS(th)}$ can be defined by several measurement methods. Examples of $V_{GS(th)}$ measurement methods are listed below:

a) Example 1: Constant current method 1 ($V_{GS(th)}$ is measured with constant V_{DS}.)

   Figure 3 and Figure 4 show schematics of the sequence of positive bias temperature instability (PBTI) test and I_{DS} versus V_{GS} curve for Example 1, respectively. The procedure of $V_{GS(th)}$ measurement is that the drain to source current (I_{DS}) is measured while sweeping gate to source voltage (V_{GS}). The drain to source voltage (V_{DS}) is kept constant to flow the I_{DS}. A threshold current ($I_{DS(th)}$) shall be defined to measure $V_{GS(th)}$. $V_{GS(th)}$ is the V_{GS} when the I_{DS} crosses the threshold current during the V_{GS} sweeping operation. A conditioning pulse is applied prior to measuring the $V_{GS(th)}$, as shown in Figure 3. The conditioning procedure is described in 5.4.

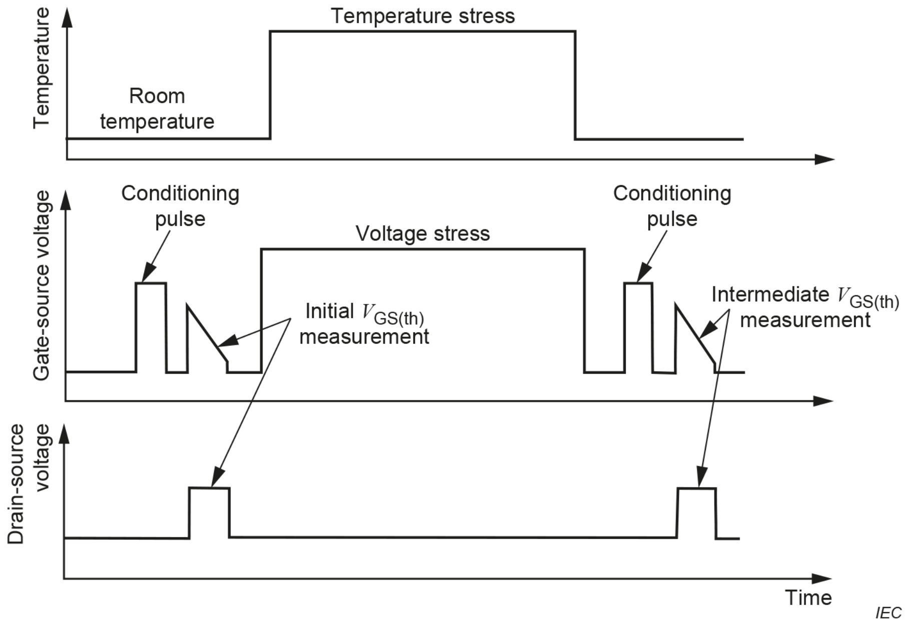


Figure 3 – Schematic of test pattern for Example 1

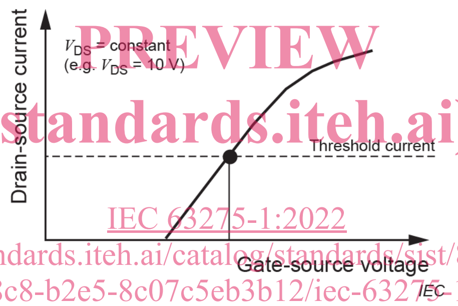


Figure 4 – I_{DS} versus V_{GS} curve for Example 1

b) Example 2: Constant current method 2 ($V_{GS(th)}$ is measured with V_{GS} = V_{DS}.)

Figure 5 and Figure 6 show schematics of the sequence of PBTI test and I_{DS} versus V_{GS} curve for Example 2, respectively. The procedure of $V_{GS(th)}$ measurement is that the I_{DS} is measured while sweeping V_{GS}. The V_{DS} is kept the same as the V_{GS} to allow the I_{DS} to flow. A threshold current $I_{DS(th)}$ shall be defined to measure $V_{GS(th)}$. $V_{GS(th)}$ is the V_{GS} when the I_{DS} crosses the $I_{DS(th)}$ during the V_{GS} sweeping operation. The I_{DS} current limit shall be set to a rated-current value corresponding to a standard scale, such as 250 µA/A (e.g. for a 20 A device, I_{DS} limit is 5 mA).

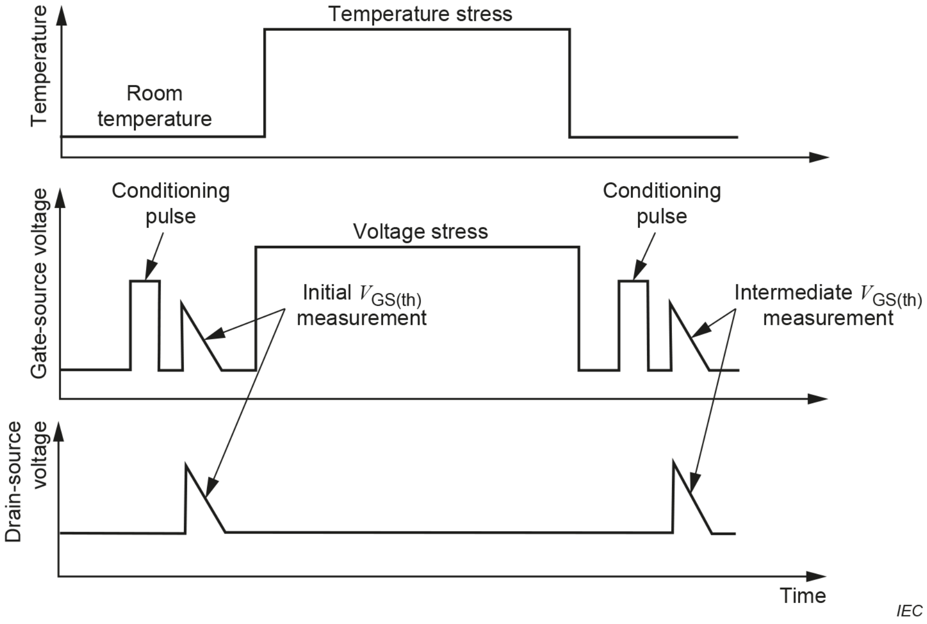


Figure 5 – Schematic of test pattern for Example 2 and Example 3

Figure 6 – I_{DS} versus V_{GS} curve for Example 2

c) Example 3: Extrapolation method

Figure 7 shows a schematic of the I_{DS} versus V_{GS} curve for Example 3. I_{DS} is measured at condition of V_{DS} = V_{GS}. $V_{GS(th)}$ is the X-intercept of the interpolated line of square root of I_{DS}.

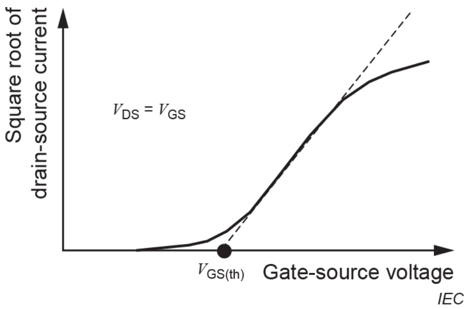


Figure 7 – I_{DS} – V_{GS} curve for Example 3