IEC 63275-2

Edition 1.0 2022-05

INTERNATIONAL STANDARD

NORME INTERNATIONALE

Semiconductor devices – Reliability test method for silicon carbide discrete metal-oxide semiconductor field effect transistors –
Part 2: Test method for bipolar degradation due to body diode operation

Dispositifs à semiconducteurs – Méthode d'essai de fiabilité pour les transistors à effet de champ métal-oxyde-semiconducteurs discrets en carbure de silicium –
Partie 2: Méthode d'essai de la dégradation bipolaire due au fonctionnement de la diode intrinsèque

IEC 63275-2:2022-05(en-fr)

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

COMMISSION ELECTROTECHNIQUE INTERNATIONALE

ICS 31.080.30

ISBN 978-2-8322-0121-3

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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Part 2: Test method for bipolar degradation due to body diode operation

FOREWORD

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The text of this International Standard is based on the following documents:

Draft	Report on voting
47/2756/FDIS	47/2765/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

A list of all parts in the IEC 63275 series, published under the general title *Semiconductor devices – Reliability test method for silicon carbide discrete metal-oxide semiconductor field effect transistors*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

INTRODUCTION

Silicon carbide (SiC) is widely used as a semiconductor material for next-generation power semiconductor devices. SiC, as compared with silicon (Si), has superior physical properties such as a higher breakdown electric field, higher thermal conductivity, lower carrier generation rate, higher saturated electron drift velocity, and lower intrinsic carrier concentration. These attributes realize SiC-based power semiconductor devices with faster switching speeds, lower losses, higher blocking voltages, and higher temperature operation relative to standard Si based power semiconductor devices.

Possible reliability issues include on-state voltage drop change, on-state resistance increase and reverse drain voltage change of metal-oxide semiconductor field effect transistors due to a current flowing through the body diode. This occurs because the body diode current causes the formation of stacking faults that expand within the drift region of the MOSFET and impede current flow within the area that they occupy. This increases the on-state resistance and degrades the operation of the power electronics system. This effect will only occur if the active device volume contains basal plane dislocations (BPDs), and there is electron-hole pair (EHP) recombination such as occurs during forward biasing of the body diode of the SiC MOSFET. That means some of the devices may show parameter drift, others will not drift. Therefore, it is indispensable to establish an International Standard with regard to evaluation of on-state voltage drop change and on-state resistance change as reliability issues.

This document defines the evaluation method of on-state voltage drop change and on-state resistance change under body diode current stress on SiC metal-oxide semiconductor field effect transistors.

SEMICONDUCTOR DEVICES – RELIABILITY TEST METHOD FOR SILICON CARBIDE DISCRETE METAL-OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTORS –

Part 2: Test method for bipolar degradation due to body diode operation

1 Scope

This part of IEC 63275 gives the test method and a procedure using this method to evaluate the on-state voltage change, on-state resistance change and reverse drain voltage change of silicon carbide (SiC) power MOSFET devices due to body diode operation. This test is not generally requested for Si power transistors.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60747-8, *Semiconductor devices – Discrete devices – Part 8: Field-effect transistors*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60747-8 and the following apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1
silicon carbide
compound semiconductor material composed of silicon and carbon

3.2
on-state voltage change
change in the on-state voltage ($V_{DS(on)}$) due to body diode current stress from the source terminal of the device to the drain terminal

3.3
on-state resistance change
change in the on-state resistance ($R_{DS(on)}$) due to body diode current stress from the source terminal of the device to the drain terminal

3.4
reverse drain voltage change
change in the reverse drain voltage (V_{SD}) due to body diode current stress from the source terminal of the device to the drain terminal

4 Method

4.1 General

The change in values of the on-state voltage, the on-state resistance and the reverse drain voltage occurs when body diode current flows through a body diode of n-channel vertical power MOSFETs fabricated on SiC crystal. This test is intended to evaluate the change in values of the on-state voltage, the on-state resistance and the reverse drain voltage under the body diode current stress on n-channel vertical power MOSFETs fabricated on SiC crystal.

4.2 Principle

This test method evaluates the change in values of $V_{DS(on)}$, $R_{DS(on)}$ and V_{SD} by alternating between conducting the measurements and applying the stress through the body diode current to the MOSFETs. The test flow chart is shown in Figure 1.

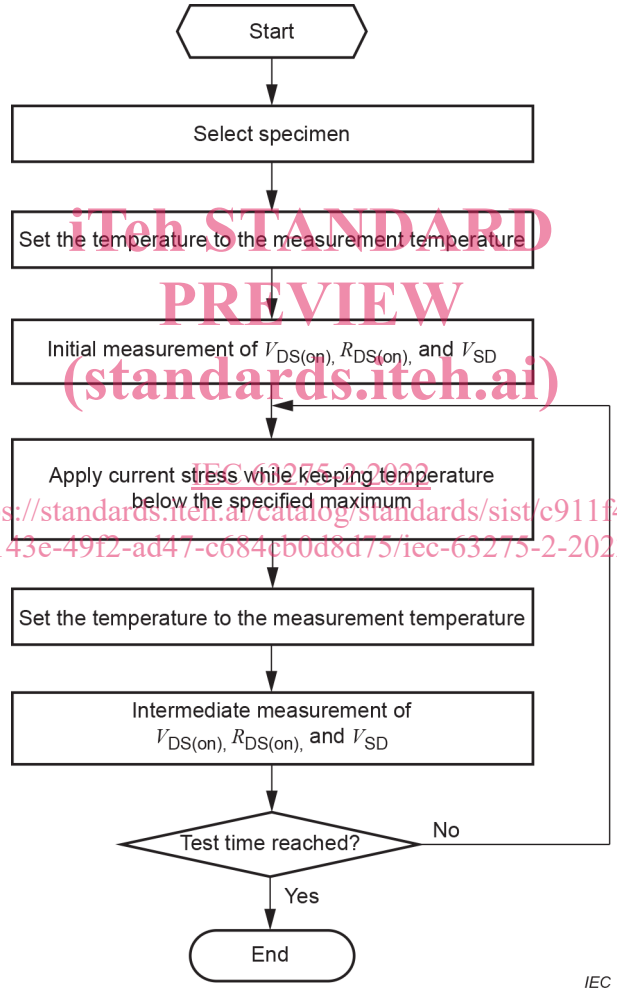


Figure 1 – Test flow chart

4.3 Requirements

4.3.1 Samples

Samples shall have the same MOSFET structure to the evaluation target product. Either the wafer-level or the package-level may be selected for the evaluation. Package-level is recommended to ensure ohmic contact to the MOSFET's electrode.

Unless otherwise specified, a minimum of four samples is recommended for each test condition to evaluate the representative behaviour of $V_{DS(on)}$, $R_{DS(on)}$ and V_{SD} change. For better statistics, a bigger sample size may be needed to ensure lower values of lot tolerance percent defect (LTPD). When the test method is applied to qualify reliability of product, the sample size should be defined by taking into consideration device-to-device deviation of change in values of $V_{DS(on)}$, $R_{DS(on)}$ and V_{SD}, and target applications of the product.

4.3.2 Test temperature

The test shall be performed at a temperature no higher than the maximum in the device specifications. The measurement temperature should be set to the same temperature for each measurement, and room temperature is recommended.

4.3.3 Test current

The test shall be performed at the rated diode forward current (if a pulsed current stress is applied, then this would be the rated pulse current; if a DC current stress is applied, then this would be the rated DC current), and at the rated case temperature and at or below the rated maximum junction temperature. In order to regulate the temperature of the sample, pulse width modulation current is recommended. V_{GS} shall be set at the rated negative voltage to prevent the MOSFET channel from conducting.

4.3.4 Test time

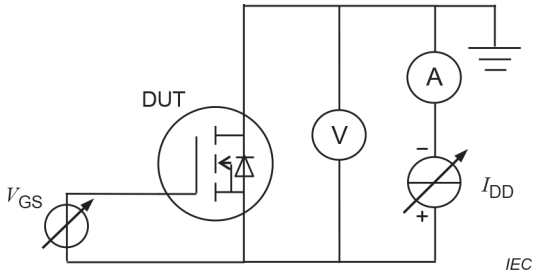
The test time shall be set individually to reach a limit of an acceptable change in values of $V_{DS(on)}$, $R_{DS(on)}$ and V_{SD}, or to collect the data required to extrapolate the time to reach a limit of the acceptable change in values of $V_{DS(on)}$, $R_{DS(on)}$ and V_{SD}. The time for temperature ramping and measuring shall not be included in the test time. Extrapolation of degradation effects shall not overestimate the actual degradation for longer stressing times if extrapolation is performed. Measuring time shall not be included in the test time.

4.3.5 Failure criteria

The failure criteria of each change in values of $V_{DS(on)}$, $R_{DS(on)}$ and V_{SD} should be a 20 % change in initial values unless there are individual specifications. In addition, the failure criteria should be linked to a maximum allowed change in the parameter value so that it does not violate the data sheet specification or cause other failures in an intended application.

4.4 Parameter setting

Figure 2 shows the test circuit. This test requires equipment that is capable of providing particular body diode current on the sample. I_{DD} is the current source to apply body diode current stress. V_{GS} is the voltage source to apply negative gate bias during current stress test on the sample.



Key

A	ammeter to measure body diode current of DUT
V	voltmeter to measure reverse drain voltage of DUT
DUT	device under test sample
V_{GS}	voltage source
I_{DD}	current source

Figure 2 – Circuit diagram for body diode current stress test

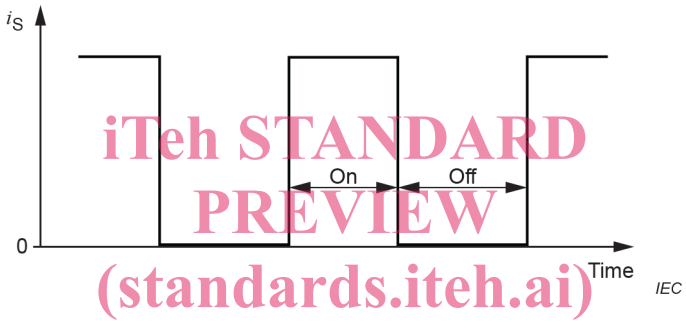


Figure 3 – Rectangular current waveform by the current source in the test circuit

4.5 Procedures

4.5.1 Setting

Set the sample in the test apparatus.

4.5.2 Ambient temperature

Set the ambient temperature to the test temperature.

4.5.3 Initial measurement

Measure the $V_{DS(on)}$, $R_{DS(on)}$ and V_{SD} of the sample at the measurement temperature.

4.5.4 Stress current

Apply the current stress to the source terminal of the sample. When a temperature rise is unacceptable in terms of current stress, a pulsed current source that generates rectangular current waveform shall be used as shown in Figure 3. The on/off ratio shall be such that the temperature rise does not exceed the rated temperature. The rise time and fall time of the rectangular current waveform shall be such that the overshoot does not exceed the maximum rating of the device. If using DC current stress, the temperature of the device shall be within the maximum ratings as the temperature of the device is likely to rise.