IEC 60191-6-10

Edition 1.0 2003-11

INTERNATIONAL STANDARD

NORME INTERNATIONALE

Mechanical standardization of semiconductor devices –
Part 6-10: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Dimensions of P-VSON

Normalisation mécanique des dispositifs à semiconducteurs –
Partie 6-10: Règles générales pour la préparation des dessins d'encombrement des dispositifs à semiconducteurs pour montage en surface – Dimensions des boîtiers P-VSON

IEC Central Office
3, rue de Varembé
CH-1211 Geneva 20
Switzerland

Tel.: +41 22 919 02 11
Fax: +41 22 919 03 00
info@iec.ch
www.iec.ch

About the IEC

The International Electrotechnical Commission (IEC) is the leading global organization that prepares and publishes International Standards for all electrical, electronic and related technologies.

About IEC publications

The technical content of IEC publications is kept under constant review by the IEC. Please make sure that you have the latest edition, a corrigenda or an amendment might have been published.

Useful links:

IEC publications search - www.iec.ch/searchpub

The advanced search enables you to find IEC publications by a variety of criteria (reference number, text, technical committee,…).
It also gives information on projects, replaced and withdrawn publications.

Electropedia - www.electropedia.org

The world's leading online dictionary of electronic and electrical terms containing more than 30 000 terms and definitions in English and French, with equivalent terms in additional languages. Also known as the International Electrotechnical Vocabulary (IEV) on-line.

IEC Just Published - webstore.iec.ch/justpublished

Stay up to date on all new IEC publications. Just Published details all new publications released. Available on-line and also once a month by email.

Customer Service Centre - webstore.iec.ch/csc

If you wish to give us your feedback on this publication or need further assistance, please contact the Customer Service Centre: csc@iec.ch.

A propos de la CEI

La Commission Electrotechnique Internationale (CEI) est la première organisation mondiale qui élabore et publie des Normes internationales pour tout ce qui a trait à l'électricité, à l'électronique et aux technologies apparentées.

A propos des publications CEI

Le contenu technique des publications de la CEI est constamment revu. Veuillez vous assurer que vous possédez l'édition la plus récente, un corrigendum ou amendement peut avoir été publié.

Liens utiles:

Recherche de publications CEI - www.iec.ch/searchpub

La recherche avancée vous permet de trouver des publications CEI en utilisant différents critères (numéro de référence, texte, comité d'études,…).
Elle donne aussi des informations sur les projets et les publications remplacées ou retirées.

Electropedia - www.electropedia.org

Le premier dictionnaire en ligne au monde de termes électroniques et électriques. Il contient plus de 30 000 termes et définitions en anglais et en français, ainsi que les termes équivalents dans les langues additionnelles. Egalement appelé Vocabulaire Electrotechnique International (VEI) en ligne.

Just Published CEI - webstore.iec.ch/justpublished

Restez informé sur les nouvelles publications de la CEI. Just Published détaille les nouvelles publications parues. Disponible en ligne et aussi une fois par mois par email.

Service Clients - webstore.iec.ch/csc

Si vous désirez nous donner des commentaires sur cette publication ou si vous avez des questions contactez-nous: csc@iec.ch.

IEC 60191-6-10

Edition 1.0 2003-11

INTERNATIONAL STANDARD

NORME INTERNATIONALE

Mechanical standardization of semiconductor devices –
Part 6-10: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Dimensions of P-VSON

Normalisation mécanique des dispositifs à semiconducteurs –
Partie 6-10: Règles générales pour la préparation des dessins d'encombrement des dispositifs à semiconducteurs pour montage en surface – Dimensions des boîtiers P-VSON

INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

COMMISSION
ELECTROTECHNIQUE
INTERNATIONALE

PRICE CODE
CODE PRIX

M

ICS 31.080.01

ISBN 978-2-83220-520-4

INTERNATIONAL ELECTROTECHNICAL COMMISSION

MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

Part 6-10: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Dimensions of P-VSON

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
5) IEC provides no marking procedure to indicate its approval and cannot be rendered responsible for any equipment declared to be in conformity with an IEC Publication.
6) All users should ensure that they have the latest edition of this publication.
7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 60191-6-10 has been prepared by subcommittee 47D: Mechanical standardization of semiconductor devices, of IEC technical committee 47: Semiconductor devices.

This bilingual version (2012-12) corresponds to the monolingual English version, published in 2003-11.

The text of this standard is based on the following documents:

FDIS	Report on voting
47D/551/FDIS	47D565/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

The French version of this standard has not been voted upon.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this publication will remain unchanged until 2005. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

Part 6-10: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Dimensions of P-VSON

1 Scope

This part of IEC 60191 provides the common outline drawings and dimensions for all types of structures and composed materials of plastic very thin small outline non-lead package (hereinafter called P-VSON).

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60191(all parts), *Mechanical standardization of semiconductor devices*

ISO/DIS 2692: *Geometrical Product Specification (GPS) – Geometrical tolerancing – Maximum material requirement (MMR) and least material requirement (LMR)*

3 Terms and definitions

For the purposes of this document, the following definition, as well as those given in other parts of the IEC 60191 series, apply.

3.1
P-VSON
plastic very thin-profile small outline, flat package with no leads

NOTE The package leads (terminals) are on opposite sides of the bottom of the package body and do not extend beyond the package body.

Drawing of Plastic non-lead packages with two parallel rows of terminals

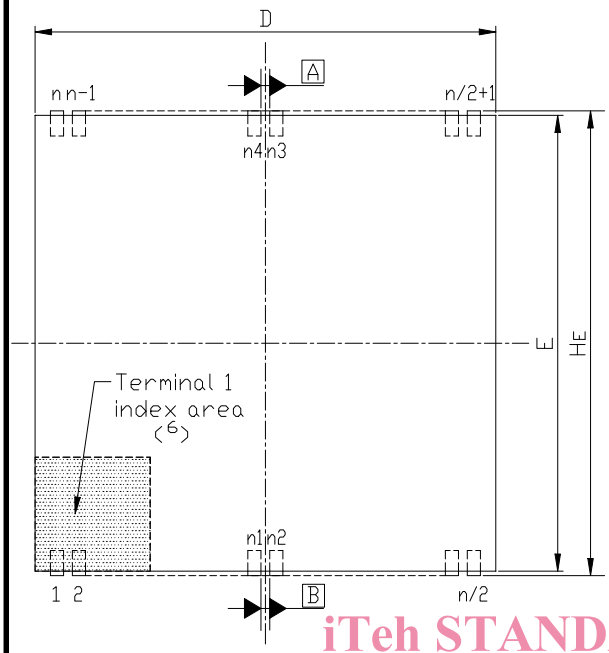


Figure 1a

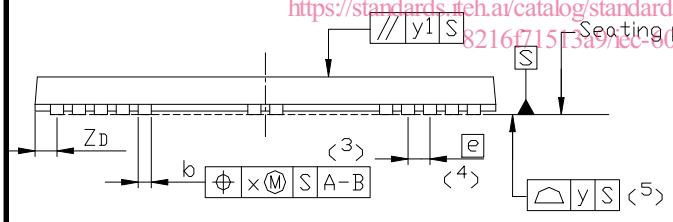


Figure 1b

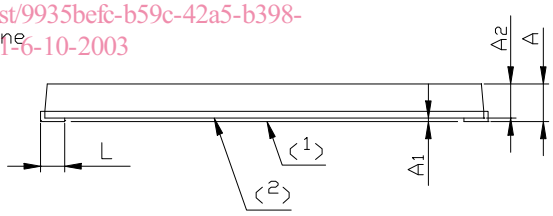
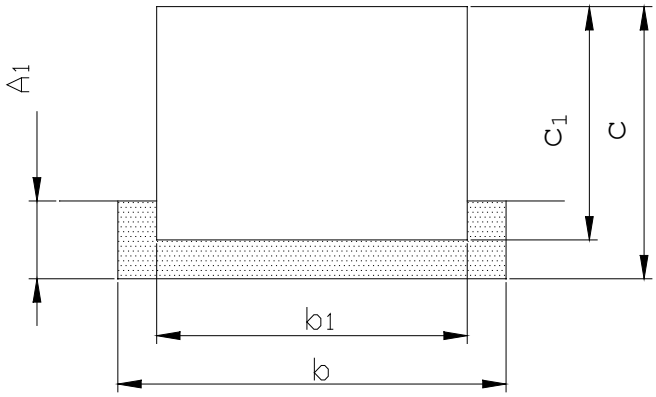


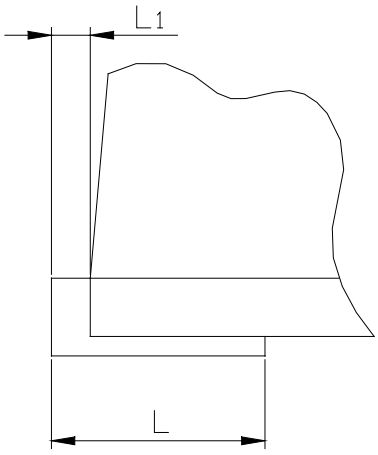
Figure 1c

Drawing of Plastic non-lead packages with two parallel rows of terminals



Terminal cross section([7])

Figure 1d



Terminal to be soldered

Figure 1e

Definition of the datum

(a) For even number of leads on a package side.

(b) For odd number of leads on a package side.

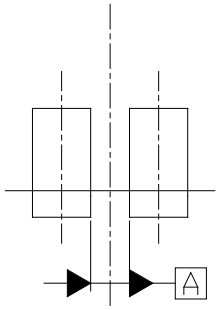


Figure 1f

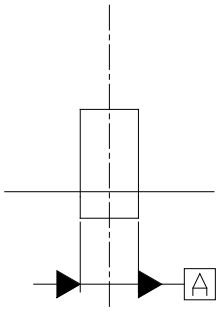
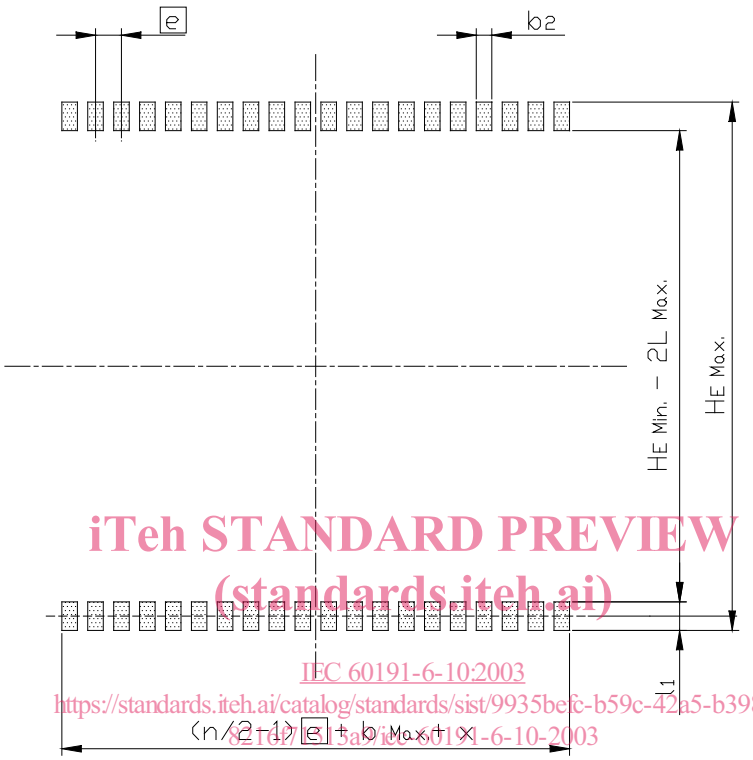


Figure 1g

The definition of datum B is the same as the definition of datum A.

Drawing of Plastic non-lead packages with two parallel rows of terminals



Pattern of terminal position areas

Figure 2

Table 1 – Dimensions to be specified for Group 1

Group 1 – Group 1 includes dimensions and numerals associated with mounting of packages and different kinds of packages. The dimensions and numerals belonging to the group mean values is guaranteed to users and imply that mechanical compatibility of mounting of packages can be recognized.

<table>
<tr><th rowspan="2">Name</th><th rowspan="2">Ref.</th><th colspan="3">Limits to be observed</th><th rowspan="2">Recommended values for the dimension
mm</th><th rowspan="2">Note</th></tr>
<tr><th>Min.</th><th>Nom.</th><th>Max.</th></tr>
<tr><td>Standard number of terminals</td><td>n</td><td>–</td><td>X</td><td>–</td><td>See Table 3</td><td>9</td></tr>
<tr><td>Seated height</td><td>A</td><td>–</td><td>–</td><td>X</td><td>A_{max} = 1,0</td><td></td></tr>
<tr><td>Stand-off height</td><td>A_1</td><td>X</td><td>–</td><td>X</td><td><table><tr><th>$A_{1\ min.}$</th><th>$A_{1\ max.}$</th></tr><tr><td>0,00</td><td>0,05</td></tr></table></td><td>7</td></tr>
<tr><td>Body height</td><td>A_2</td><td>–</td><td>X</td><td>–</td><td>$A_{2\ nom.}$ = 0,75</td><td></td></tr>
<tr><td>Terminal width plated</td><td>b</td><td>X</td><td>–</td><td>X</td><td><table><tr><th>e</th><th>$b_{min.}$</th><th>$b_{max.}$</th></tr><tr><td>1,25</td><td>0,55</td><td>0,70</td></tr><tr><td>1,00</td><td>0,55</td><td>0,70</td></tr><tr><td>0,80</td><td>0,35</td><td>0,50</td></tr><tr><td>0,65</td><td>0,30</td><td>0,45</td></tr><tr><td>0,50</td><td>0,25</td><td>0,40</td></tr><tr><td>0,40</td><td>0,15</td><td>0,25</td></tr></table></td><td>7</td></tr>
<tr><td>Terminal thickness plated</td><td>c</td><td>X</td><td>–</td><td>X</td><td><table><tr><th>$c_{min.}$</th><th>$c_{max.}$</th></tr><tr><td>0,09</td><td>0,25</td></tr></table></td><td></td></tr>
<tr><td>Package length</td><td>D</td><td>X</td><td>X</td><td>X</td><td>From 7,00 to 26,00 increment 1,00
$D_{max.} = D_{nom.} + 0,20$
$D_{min.} = D_{nom.} - 0,20$</td><td></td></tr>
<tr><td>Package width</td><td>E</td><td>X</td><td>X</td><td>X</td><td>$E_{nom.}$ From 5,00 to 13,00 increment 1,00
$E_{max.} = E_{nom.} + 0,20$
$E_{min.} = E_{nom.} - 0,20$</td><td></td></tr>
<tr><td>Terminal pitch</td><td>e</td><td>–</td><td>X(*)</td><td>–</td><td>$e_{nom.}$ =1,25;1,00; 0,80; 0,65; 0,50; 0,40</td><td>4</td></tr>
<tr><td>Overall width</td><td>H_E</td><td>X</td><td>X</td><td>X</td><td>$H_E = E + 2L_{1\ nom.}$</td><td></td></tr>
</table>

Table 1 *(continued)*

<table>
<tr><th rowspan="2">Name</th><th rowspan="2">Ref.</th><th colspan="3">Limits to be observed</th><th rowspan="2">Recommended values for the dimension
mm</th><th rowspan="2">Note</th></tr>
<tr><th>Min.</th><th>Nom.</th><th>Max.</th></tr>
<tr><td>Length of solder part</td><td>L</td><td>X</td><td>–</td><td>X</td><td><table><tr><th>e</th><th>$L_{min.}$</th><th>$L_{max.}$</th></tr><tr><td>1,25</td><td>0,70</td><td>1,30</td></tr><tr><td>1,00</td><td>0,70</td><td>1,20</td></tr><tr><td>0,80</td><td>0,50</td><td>0,90</td></tr><tr><td>0,65</td><td>0,40</td><td>0,80</td></tr><tr><td>0,50</td><td>0,35</td><td>0,75</td></tr><tr><td>0,40</td><td>0,35</td><td>0,75</td></tr></table></td><td></td></tr>
<tr><td>Terminal position tolerance</td><td>x</td><td>–</td><td>–</td><td>X</td><td>$X_{max.}$ = 0,05</td><td>3</td></tr>
<tr><td>Coplanarity</td><td>y</td><td>–</td><td>–</td><td>X</td><td>$y_{max.}$ = 0,05</td><td>5</td></tr>
<tr><td>Flatness</td><td>y_1</td><td>–</td><td>–</td><td>X</td><td>$y_{1\ max.}$ = 0,10</td><td></td></tr>
</table>

.