# IEC 61189-2-808

Edition 1.0 2024-04

# INTERNATIONAL STANDARD

# NORME INTERNATIONALE

colour inside

## Test methods for electrical materials, printed board and other interconnection structures and assemblies –
## Part 2-808: Thermal resistance of an assembly by thermal transient method

## Méthodes d'essai pour les matériaux électriques, les cartes imprimées et autres structures et assemblages d'interconnexion –
## Partie 2-808 : Résistance thermique d'un assemblage par la méthode du transitoire thermique

IEC 61189-2-808:2024-04(en-fr)

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# TEST METHODS FOR ELECTRICAL MATERIALS, PRINTED BOARD AND OTHER INTERCONNECTION STRUCTURES AND ASSEMBLIES –

## Part 2-808: Thermal resistance of an assembly by thermal transient method

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The text of this International Standard is based on the following documents:

| Draft | Report on voting |
|---|---|
| 91/1935/FDIS | 91/1955/RVD |

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

A list of all parts in the IEC 61189 series, published under the general title *Test methods for electrical materials, printed board and other interconnection structures and assemblies*, can be found on the IEC website.

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# TEST METHODS FOR ELECTRICAL MATERIALS, PRINTED BOARD AND OTHER INTERCONNECTION STRUCTURES AND ASSEMBLIES –

## Part 2-808: Thermal resistance of an assembly by thermal transient method

## 1 Scope

This part of IEC 61189 describes the thermal transient method to characterize the thermal resistance of an assembly consisting of a heat source (e.g. power device), an attachment material (e.g. solder) and a dielectric layer with electrode. This method is suitable to determine the thermal resistance of materials and assembly methods as well as to optimize the thermal flux to a heat sink.

NOTE This method is not intended to measure and specify the value of the thermal resistance of a dielectric material. For that purpose, other standards exist. Examples are given in Annex A.

## 2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60194-2, *Printed boards design, manufacture and assembly – Vocabulary – Part 2: Common usage in electronic technologies as well as printed board and electronic assembly technologies*

## 3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60194-2 apply.

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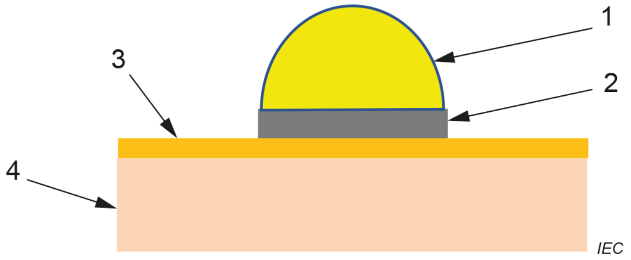
## 4 Objective

The increasing power consumption of devices such as LED require a close examination of the heat dissipating path within thermal conductive printed circuit boards (Annex A). Therefore, effective removal of heat to maintain a safe junction temperature is the key to meeting the heat flux by using thermal conductive material for printed circuit boards. Thermal resistance is the crucial factor of heat dissipation dielectric materials in printed circuit board. Therefore, with the aim to reduce the thermal resistance in circuit boards, it is proposed to determine the thermal resistance by measuring the thermal transient characteristics of an assembly.

## 5 Test specimen

To test the thermal resistance of an assembly, at first a test specimen shall be built, which consists of a heat source (e.g. power device), an attachment material (e.g. solder) and a dielectric layer with metal electrode. See Figure 1 for the structure. In the next step, the thermal resistance of the assembly can be determined by comparison of the thermal transient characteristics obtained when testing the assembly attached to a thermostat with or without a thermal interface material (TIM). See Figure 3 and Clause 6 for the test description.



**Key**

1 Heat source

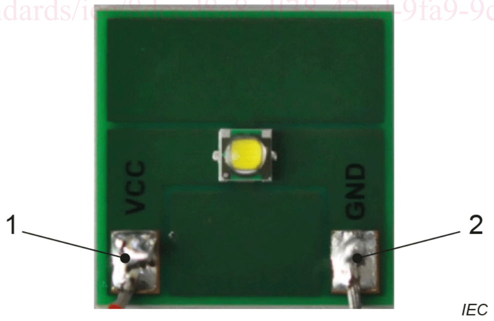
2 Solder

3 Electrode layer

4 Dielectric layer

**Figure 1 – Structure of an assembly**

To obtain an adequate thermal resistance, a layer of around 200 µm thick solder shall be used for the die attach. The power source is a chip type device of the size 3,45 mm × 3,45 mm, powered with 1 W through voltage common collector (VCC) and ground (GND). The dielectric layer is a 2 cm × 2 cm substrate of 1 mm thickness. Figure 2 shows an example of such a test specimen.



**Key**

1 Voltage common collector (VCC)

2 Ground (GND)

**Figure 2 – The fabricated test sample**

# 6 Test equipment and procedures

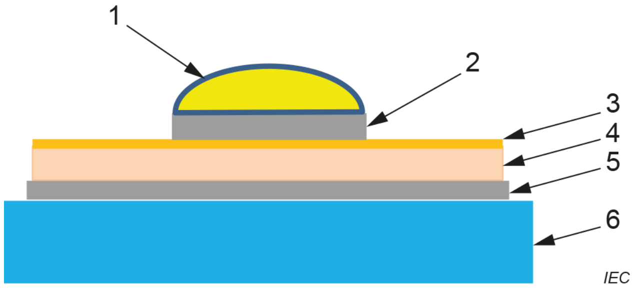
## 6.1 Test method and recommended test parameters

The thermal transient test equipment is a unique equipment for performing thermal measurements on semiconductor devices like ICs, transistors, diodes, etc. The thermal transient test equipment is most suitable for analyzing their thermal behavior, evaluating packages and device mounting, and detecting defects. This equipment is a computer-controlled equipment that can be used along with a PC hosting a special control and evaluation software. This equipment as a mandatory part of configuration can apply programmed thermal excitations and record complex thermal responses and provides built-in results evaluation procedures. Results of these post-processing procedures include the pulse thermal resistance diagram, time-constant spectrum, complex locus of the thermal impedance, differential and integral structure or profile function (Annex B).

## 6.2 Test equipment

The thermal transient measurements can be performed using a commercially available test equipment and specifically built test fixtures (Annex C). The test sample is mounted on the temperature-controlled heat sink. The heat sink is maintained at a temperature of 25 °C and controlled by a Keithley temperature controller. Initially, a junction-to-case thermal equilibrium is ensured by applying a drive current ($I_{\text{drive}}$) for a sufficiently long duration; then the $I_{\text{drive}}$ is switched off and a small sense current ($I_{\text{sense}}$) is applied. When the system shifts to its new thermal equilibrium, the cooling down of the junction is measured.

From the transient time curves, the duration of cooling down can be taken to be how long the heating current $I_{\text{drive}}$ needs to be applied to load the thermal capacities. The same time must be measured applying $I_{\text{sense}}$ to resolve the thermal path downstream to the respective capacity. One approach to determine the required measurement time is to modify the thermal interface between the heat sink and the module. The time value at which the curve with the best possible thermal interface and one with a bad thermal interface separate is approximately the appropriate time duration for $I_{\text{drive}}$ and $I_{\text{sense}}$ when the thermal path upstream of the varied thermal interface is to be investigated. One can stepwise shorten the heat-up and cool-down time afterward and observe at what setting, and at which time, values change in the logarithmic time-derived curve. The shortest time for which the deviation of the time curves is still within the signal-to-noise range of the curve with long heating and cooling times is still acceptable. The thermal response at initial ‘0’ cycles and after '$n$' cycles was measured. The measurement time of 40 s is unnecessarily long. For the second test run with test samples B, the measurement time was reduced to 5 s. In principle, this allowed us to reduce the heating up and cooling down time further to 0,5 s, because data later than 300 ms are not included for data analysis. The shape of the transient signal does not change when the cycle of heating up and cooling down times is shortened. In this experiment, the thermal tape (thermal conductivity: 6,5 W/mK) with the thickness of 500 µm is used. Thermal tape as a thermal interface material is used for separating the interface of the test sample through the comparison of thermal transient characteristics depending on whether or not the test sample has thermal interface material.



**Key**

| | |
|---|---|
| 1 | Heat source (1 W) |
| 2 | SAC305 solder (T: 200 µm) |
| 3 | Electrode layer (T: 35 µm) |
| 4 | Dielectric layer (T: 500 µm) |
| 5 | Thermal interface material (T: 500 µm) |
| 6 | Thermostat |

NOTE The thermostat is the temperature-controlled system (Annex D). The thermostat has the thermocouples inside system.

**Figure 3 – Test structure for measuring thermal resistance**

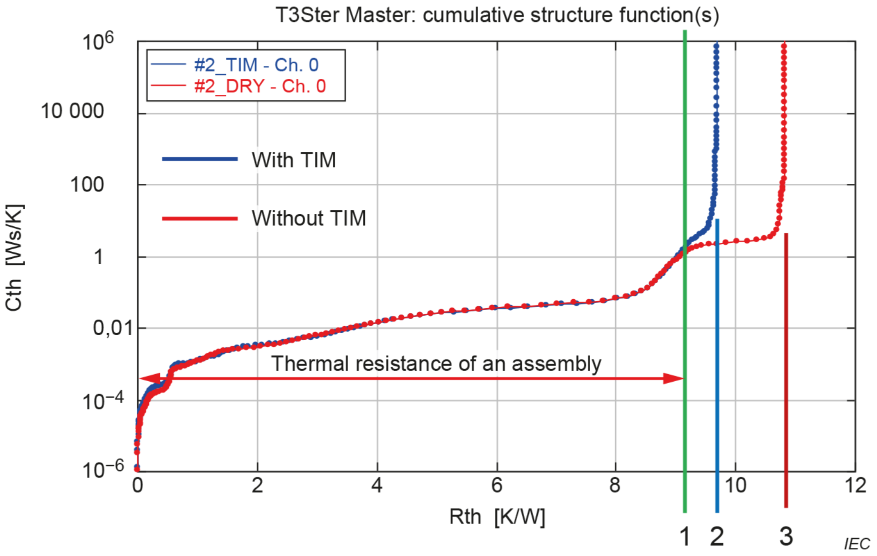
### 6.3 Test procedure

The test sequences to test the thermal resistance of an assembly are as follows:

1) cleaning the contamination on the thermostat;
2) firstly, attaching the test sample on the thermostat without the thermal interface material;
3) testing the thermal transient characteristics of the test sample by biasing the power;
    - driving current ($I_{\text{drive}}$): 1 500 mA
    - sensor current ($I_{\text{sense}}$) for test: 10 mA
    - total power: 4,548 W
    - TIM: thermal pad (thickness: 500 µm)
    - temperature coefficient: −1,272 mV/°C
4) repeat the sequence 1);
5) secondly, attaching the test sample on the thermostat by using thermal interface material;
6) testing the thermal transient characteristics of the test sample by biasing the power;
7) comparing the thermal transient characteristics of the test sample depending on with or without the thermal interface material;
8) extracting the thermal resistance value of an assembly with test results.

## 7 Test result

From the cumulative structure function of the thermal transient characteristics, after converting to the cumulative structure function because it is eased to look for the separation point, the thermal resistance value is extracted by looking for the separated point from the measurement excel sheet instead of the visible graph (see Figure 4 and Table 1). Detailed information can be found in JESD-51-14(Published: Nov 2010), clause 4, Junction-to-Case Thermal Resistance Measurement (Test Method).



**Key**

1 The measured of thermal resistance of an assembly

2 The measured thermal resistance of assembly without TIM

3 The measured thermal resistance of assembly with TIM

NOTE $C_{th}$ is thermal capacitance and K is temperature (Kelvin).

**Figure 4 – Test result for thermal resistance of an assembly**

In order to extract value for thermal resistance of assembly, the separated value from the measurement results, depending on with TIM and without TIM, should be looked for.

**Table 1 – Test result for thermal resistance of an assembly**

| **Total thermal resistance (without TIM)**<br>K/W | **Total thermal resistance (with TIM)**<br>K/W | **Thermal resistance of an assembly**<br>K/W |
|---|---|---|
| 10,86 | 9,68 | 9,2 |

## 8 Report

This test report shall include:

a) structure of the test specimen;

b) thermal tape used as TIM;

c) the used power sources;

d) the date of the test;

e) the room temperature under which the test was conducted;

f) the test sequences;

g) the graph of the cumulative structure function;

h) the total thermal resistance of the test specimen with or without TIM;

i) the thermal resistance of an assembly.

The result value of an assembly separated differently from the measurement results, depending on the presence or absence of TIM, is defined as the thermal resistance and assembly. Detailed information can be found in JESD-51-14 (Published: Nov 2010), clause 4, Junction-to-Case Thermal Resistance Measurement (Test Method).