# IEC 60749-28

Edition 2.0 2022-03

# INTERNATIONAL STANDARD

# NORME INTERNATIONALE

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## Semiconductor devices – Mechanical and climatic test methods – Part 28: Electrostatic discharge (ESD) sensitivity testing – Charged device model (CDM) – device level

## Dispositifs à semiconducteurs – Méthodes d'essais mécaniques et climatiques – Partie 28: Essai de sensibilité aux décharges électrostatiques (DES) – Modèle de dispositif chargé (CDM) – niveau du dispositif

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IEC Secretariat
3, rue de Varembé
CH-1211 Geneva 20
Switzerland

Tel.: +41 22 919 02 11
info@iec.ch
www.iec.ch

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IEC 60749-28 has been prepared by IEC technical committee 47: Semiconductor devices, in collaboration with IEC technical committee 101: Electrostatics. It is an International Standard.

ANSI/ESDA/JEDEC JS-002-2018 has served as a basis for the elaboration of this standard. It is used with permission of the copyright holders, ESD Association and JEDEC Solid state Technology Association. ANSI/ESDA/JEDEC JS-002-2018 describes the field-induced (FI) method. An alternative, the direct contact (DC) method (not based on JS-002-2018), is described in Annex J.

This second edition cancels and replaces the first edition published in 2017. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

a) a new subclause and annex relating to the problems associated with CDM testing of integrated circuits and discrete semiconductors in very small packages;

b) changes to clarify cleaning of devices and testers.

The text of this International Standard is based on the following documents:

| Draft | Report on voting |
|---|---|
| 47/2746/FDIS | 47/2754/RVD |

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

A list of all parts in the IEC 60749 series, published under the general title *Semiconductor devices – Mechanical and climatic test methods*, can be found on the IEC website.



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- withdrawn,
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- amended.



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# INTRODUCTION

The earliest electrostatic discharge (ESD) test models and standards simulate a charged object approaching a device and discharging through the device. The most common example is IEC 60749-26, the human body model (HBM). However, with the increasing use of automated device handling systems, another potentially destructive discharge mechanism, the charged device model (CDM), becomes increasingly important. In the CDM, a device itself becomes charged (e.g. by sliding on a surface (tribocharging) or by electric field induction) and is rapidly discharged (by an ESD event) as it closely approaches a conductive object. A critical feature of the CDM is the metal-metal discharge, which results in a very rapid transfer of charge through an air breakdown arc. The CDM test method also simulates metal-metal discharges arising from other similar scenarios, such as the discharging of charged metal objects to devices at different potential.

Accurately quantifying and reproducing this fast metal-metal discharge event is very difficult, if not impossible, due to the limitations of the measuring equipment and its influence on the discharge event. The CDM discharge is generally completed in a few nanoseconds, and peak currents of tens of amperes have been observed. The peak current into the device will vary considerably depending on a large number of factors, including package type and parasitics. The typical failure mechanism observed in MOS devices for the CDM model is dielectric damage, although other damage has been noted.

The CDM charge voltage sensitivity of a given device is package dependent. For example, the same integrated circuit (IC) in a small area package can be less susceptible to CDM damage at a given voltage compared to that same IC in a package of the same type with a larger area. It has been shown that CDM damage susceptibility correlates better to peak current levels than charge voltage.

# SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

## Part 28: Electrostatic discharge (ESD) sensitivity testing – Charged device model (CDM) – device level

## 1 Scope

This part of IEC 60749 establishes the procedure for testing, evaluating, and classifying devices and microcircuits according to their susceptibility (sensitivity) to damage or degradation by exposure to a defined field-induced charged device model (CDM) electrostatic discharge (ESD). All packaged semiconductor devices, thin film circuits, surface acoustic wave (SAW) devices, opto-electronic devices, hybrid integrated circuits (HICs), and multi-chip modules (MCMs) containing any of these devices are to be evaluated according to this document. To perform the tests, the devices are assembled into a package similar to that expected in the final application. This CDM document does not apply to socketed discharge model testers. This document describes the field-induced (FI) method. An alternative, the direct contact (DC) method, is described in Annex J.



The purpose of this document is to establish a test method that will replicate CDM failures and provide reliable, repeatable CDM ESD test results from tester to tester, regardless of device type. Repeatable data will allow accurate classifications and comparisons of CDM ESD sensitivity levels.

## 2 Normative references



There are no normative references in this document.

## 3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

**3.1**
**CDM ESD**
charged device model electrostatic discharge
electrostatic discharge (ESD) using the charged device model (CDM) to simulate the actual discharge event that occurs when a charged device is quickly discharged to another object at a lower electrostatic potential through a single pin or terminal

**3.2**
**CDM ESD tester**
charged device model electrostatic discharge tester
equipment that simulates the device level CDM ESD event using the non-socketed test method

Note 1 to entry: "Equipment" is referred to as "tester" in this document.

**3.3**
**$C_{Small}$**
device to CDM field plate capacitance for an integrated circuit or discrete semiconductor at or below which it has been determined that CDM testing is not required if specified conditions are met

**3.4**
**dielectric layer**
thin insulator placed atop the field plate used to separate the device from the field plate

**3.5**
**field plate**
conductive plate used to elevate the potential of the device under test (DUT) by capacitive coupling

Note 1 to entry: See Figure 1.

**3.6**
**ground plane**
conductive plate used to complete the circuitry for grounding/discharging the DUT

Note 1 to entry: See Figure 1.

**3.7**
**software voltage**
user/operator-entered voltage that, when combined with the scale factor or offset, sets the actual field plate voltage on the system in order to achieve the waveform parameters

Note 1 to entry: Waveform parameters are defined in Table 1 or Table 2.



**3.8**
**test condition**
**TC**
tester plate voltage that meets the waveform parameter conditions



Note 1 to entry: The waveform parameter conditions are found in a particular column of Table 1 and Table 2.

## 4 Required equipment

### 4.1 CDM ESD tester

#### 4.1.1 General

Figure 1 represents the hardware schematic for a CDM tester setup to conduct field-induced CDM ESD testing assuming the use of a resistive current probe. The DUT may be an actual device or it may be one of the two verification modules (metal discs) described in Annex A. The pogo pin shall be connected to the ground plane with a 1 Ω current path with a minimum bandwidth (BW) of 9 gigahertz (GHz). The 1 Ω pogo pin to ground connection of the resistive current sensor may be a parallel combination of a 1 Ω resistor between the pogo pin and the ground plane, and the 50 Ω impedance of the oscilloscope and its coaxial cable. In Figure 1, K1 is the switch between charging the field plate and grounding the field plate. The CDM ESD testers used within the context of this document shall meet the waveform characteristics specified in Figure 2, and Table 1 and Table 2, without additional passive or active devices, such as ferrites, in the probe's assembly.

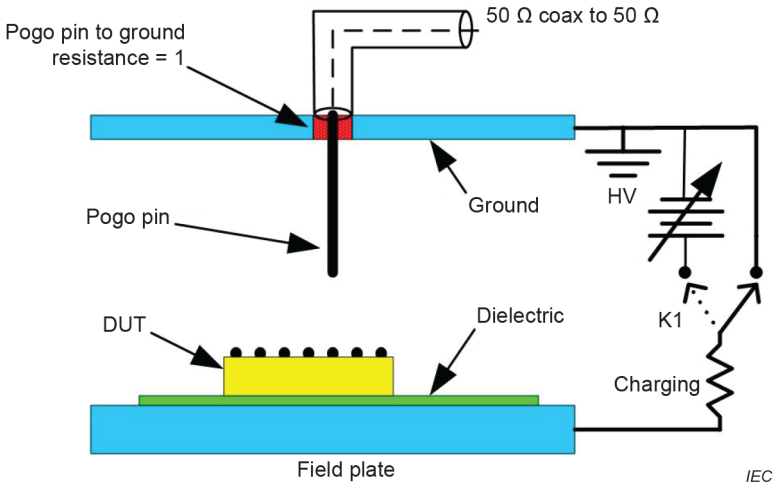


**Figure 1 – Simplified CDM tester hardware schematic**

When constructing the test equipment, the parasitics in the charge and discharge paths should be minimized since the resistance inductance-capacitance (RLC) parasitics in the equipment greatly influence the test results.

For existing equipment, it is recommended to contact qualified service personnel to determine compliance to this document upon removal of ferrite components.



### 4.1.2 Current-sensing element

A current-sensing element shall be incorporated into the ground plane. The resistance of this element shall have a value of (1,0 ± 10 %) Ω. A resistor, as specified in 4.1.1, shall be used as the current-sensing element. The value of resistance (including the 50 Ω cable/oscilloscope termination) shall be measured using an ohmmeter as described in 4.5. The resistance value shall be used to calculate the first peak current.



The current-sensing element shall have a minimum frequency response of 9 GHz (specified by a maximum roll-off of 3 dB at 9 GHz).

### 4.1.3 Ground plane

The probe assembly shall contain a square ground plane with the probe pin centred within it as shown in Figure 1. The dimensions of the ground plane shall be 63,5 mm × 63,5 mm ± 6,35 mm (2,5 inches × 2,5 inches ± 0,25 inches).

### 4.1.4 Field plate/field plate dielectric layer

The field plate shall have a surface flatness to vary no more than ± 0,127 mm (0,005 inches). The field plate dielectric layer should be made with an FR4 or similar epoxy-glass material. For FR4, the thickness and thickness tolerance of this dielectric layer should be 0,381 mm ± 0,0254 mm (0,015 inches ± 0,001 inches) in order to result in a capacitance measurement (as specified in normative Annex B) in the range specified in Table A.1.

If a different material is used, the material thickness is chosen to result in a capacitance measurement in the range specified in Table A.1.

### 4.1.5 Charging resistor

The charging resistor shown in Figure 1 shall nominally be 100 MΩ or greater.

Resistor values higher than 100 MΩ may be used, but this may not allow very large devices (refer to 5.9 and Annex I) to charge fully before being discharged by the probe assembly. This effect can be overcome by adding a delay between discharges in the CDM tester programming software. If using a resistor greater than 100 MΩ, it is recommended that the tester or the device itself be characterized to determine if a delay is needed for discharging large devices. A procedure for this large device delay characterization is given in Annex I.

## 4.2 Waveform measurement equipment

### 4.2.1 General

The CDM waveform measurement equipment shall consist of the following components.

### 4.2.2 Cable assemblies

Cable assemblies with combined internal tester cable and external cable total loss of no more than 2 dB at frequencies up to 5 GHz and a nominal 50 Ω impedance.

### 4.2.3 Equipment for high-bandwidth waveform measurement

#### 4.2.3.1 High-bandwidth oscilloscope

An oscilloscope or transient digitizer with a minimum real-time (single shot) 3 dB BW of at least 6 GHz and ≥ 20 gigasample/s sampling rate with a nominal 50 Ω input impedance.



#### 4.2.3.2 Attenuator

A 20 dB attenuator with a precision of ±0,5 dB, at least 12 GHz BW, and an impedance of 50 Ω ± 5,0 Ω.

### 4.2.4 Equipment for 1,0 GHz waveform measurement



#### 4.2.4.1 1 GHz oscilloscope

An oscilloscope or transient digitizer with a real-time (single shot) 3 dB BW of 1 GHz with a nominal 50 Ω input impedance. The sampling rate shall be ≥ 5 gigasample/s.

NOTE The user has the option of using a higher BW oscilloscope and using a hardware or software filter to produce a bandwidth and sampling rate equivalent to that specified in 4.2.4.1.

#### 4.2.4.2 Attenuator

A 20 dB attenuator with a precision of ± 0,5 dB, at least 4 GHz BW, and an impedance of 50 Ω ± 5 Ω.

## 4.3 Verification modules (metal discs)

The large verification module shall have a capacitance of (55 ± 5 %) pF and the small verification module shall have a capacitance of (6,8 ± 5 %) pF. Refer to normative Annex A for information on the verification module physical dimensions and normative Annex B for information on the capacitance measurement procedure.

## 4.4 Capacitance meter

Capacitance meter with a resolution of 0,2 pF, a measurement accuracy of 3 %, and a measurement frequency of 1,0 MHz as described in normative Annex B.

## 4.5 Ohmmeter

The ohmmeter used to measure the resistance of the resistive probe shall be capable of measuring to an accuracy of 0,01 Ω. Use of Kelvin 4-wire connections is recommended.

# 5 Periodic tester qualification, waveform records, and waveform verification requirements

## 5.1 Overview of required CDM tester evaluations

The CDM tester shall be qualified, re-qualified, and periodically verified as described in 5.5 and 5.6.

NOTE 1 Dielectric layers, ground planes (ground plates), the coaxial discharging resistor (probe), the distance between the ground plane and the field plate, the verification modules and the discharge contacts (e.g., pogo pins) are key elements of the tester construction. Any change to these elements necessitates a waveform verification.

NOTE 2 Changes in the shape of the discharge pulse, even though they can still be within specification, can indicate degradation of the discharge path.

## 5.2 Waveform capture hardware

Waveform capture requires the following instrumentation and tester set voltage procedure:

- an oscilloscope as specified in 4.2;
- an attenuator and cable assembly as defined in 4.2;
- verification modules (as described in 4.3) with the dimensions and attributes listed in normative Annex A and the method of measurement listed in normative Annex B.

## 5.3 Waveform capture setup



The waveform capture setup shall be carried out as follows:

a) Clean the verification modules. Avoid skin contact with the modules prior to, and during testing. A recommended procedure is described in normative Annex A.

b) Using an alcohol wipe, clean the discharge probe and the field charge plate on which the device is placed to remove any surface contamination that could result in charge loss. Ensure the pogo pin is free of particulates.



c) Attach the appropriate 20 dB attenuator as described in 4.2.3.2 to the oscilloscope. Attach one end of the external cable assembly, as described in 4.2.2, to the attenuator and the other end to the CDM tester. Verify all connections in the measurement chain are tight.

See informative Annex F for an example of oscilloscope settings and captured waveforms.

## 5.4 Waveform capture procedure

The waveform capture procedure shall be carried out as follows:

a) Place the verification module to be used on the field plate dielectric, ensuring intimate contact between the field plate dielectric and verification module.

b) Set the potential of the field plate to the needed voltage for the test condition being run.

c) Align the ground pin to approximately the centre of the verification module.

d) Either the single discharge or dual discharge method as described in Clause G.2 or Clause G.3 respectively can be used, but the discharge method chosen should be consistent with how products will be tested. When using the dual discharge method, waveforms for positive and negative pulses require a change in the oscilloscope trigger conditions to capture only positive or negative pulses.

e) Discharge the verification module at least ten times at the polarity being verified.

f) Observe at least ten successive waveforms during the set of discharges above and record the average waveform parameters for $I_p$, $T_r$, full width at half maximum (FWHM), and Ip2 for this group of waveforms as shown in Figure 2.