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TECHNICAL REPORT

colour inside

Device embedding assembly technology – Part 2-8: Guidelines – Warpage control of active device embedded substrate

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CONTENTS

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DEVICE EMBEDDING ASSEMBLY TECHNOLOGY –

Part 2-8: Guidelines – Warpage control of active device embedded substrate

FOREWORD

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IEC TR 62878-2-8, which is a technical report, has been prepared by IEC technical committee 91: Electronics assembly technology.

The text of this Technical Report is based on the following documents:

Draft	Report on voting
91/1649/DTR	91/1721/RVDTR

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this Technical Report is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

A list of all parts in the IEC 62878 series, published under the general title *Device embedding assembly technology*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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DEVICE EMBEDDING ASSEMBLY TECHNOLOGY –

Part 2-8: Guidelines – Warpage control of active device embedded substrate

1 Scope

This part of IEC 62878 describes a warpage control of active device embedded substrate along with parameters for determining warpage, which are useful during package assembly. Warpage results are explained using warpage driving force, resistance and neutral axis, for typical die embedded substrate, where the discrete active dies are placed in the core of substrate and interconnected to the substrate by direct Cu bonding. The same principles are applicable in other device embedded substrates. Even though the detailed structure of other device embedded substrates might be different, the origin and determination of the parameters of warpage are the same and thus the purpose of this report is to help engineers improve the warpage behaviours of their products by applying this principle.

2 Normative references

IEC 60194 (all parts), *Printed boards design, manufacture and assembly – Vocabulary*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60194 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1
warpage
deviation from uniform flatness of the substrate for the range of thermal conditions experienced during the package to board assembly

Note 1 to entry: Warpage during board assembly can cause the device terminals to have open or short circuit connections after the reflow soldering operation. Certain package types, such as BGAs (ball grid arrays), have been found to be more susceptible to component warpage [1][1].

Note 2 to entry: Package warpage depends on many factors including CTE mismatch between device constituents, assembly process, package design geometries, top and embedded die, substrate, etc. (x, y, & z). In addition, it can be related with use of IHS (integrated heat spreader), stiffener, or overmold (geometries and material choices include sealant/adhesives used), and other technology aspects of embedded design, embedded and external caps, use of GaA vs. SiO2, etc.

[1] Numbers in square brackets refer to the Bibliography.

4 Warpage driving force and resistance

4.1 General

Warpage of device embedded substrate can be related with many parameters which include properties, thickness, Cu ratio, routing and process history. The dimensions of embedded die including thickness, affect the warpage as well. Process history adds some variations by altering the material properties, and the residual stresses of constituents or interfaces between constituents. These parameters can be categorized into two groups, driving force and resistance.

4.2 Warpage driving force

The degree of warpage of device embedded substrate is proportional to the difference in CTE(coefficient of thermal expansion) of the materials and also to the temperature increase.

$$W \propto \Delta\alpha\Delta T$$

W: the degree of the warpage;

$\Delta\alpha$: the difference between the materials CTEs;

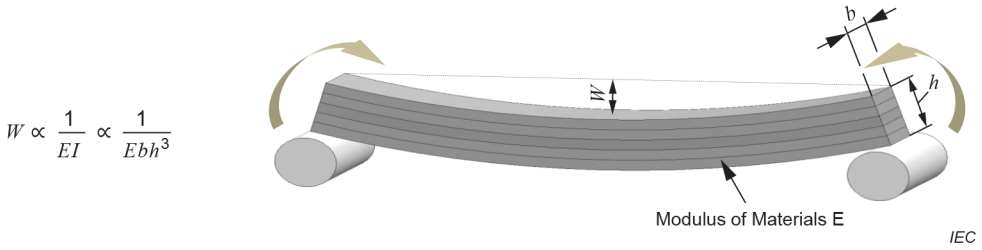
ΔT: the amount of the temperature change.

The direction of warpage can be defined by the direction of temperature change as Figure 1.

Figure 1 – Warpage behaviour of device embedded substrate during heating and cooling

4.3 Warpage resistance

Device embedded substrate warpage is inversely proportional to flexural rigidity, which is the Young's Modulus multiplied by geometrical moment of inertia. In case of the panel with fixed width of the beam (b), the warpage is proportional to the inverse of the panel thickness to the third power as shown in Figure 2.



Key

W: amount of the warpage;

E: Young's modulus;

I: geometrical moment of inertia;

EI: flexural rigidity;

b: width of the beam;

h: height of the beam.

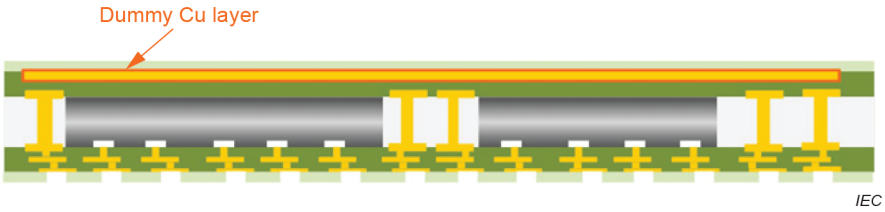
Figure 2 – Relationship between warpage and rigidity

4.4 Determining parameters

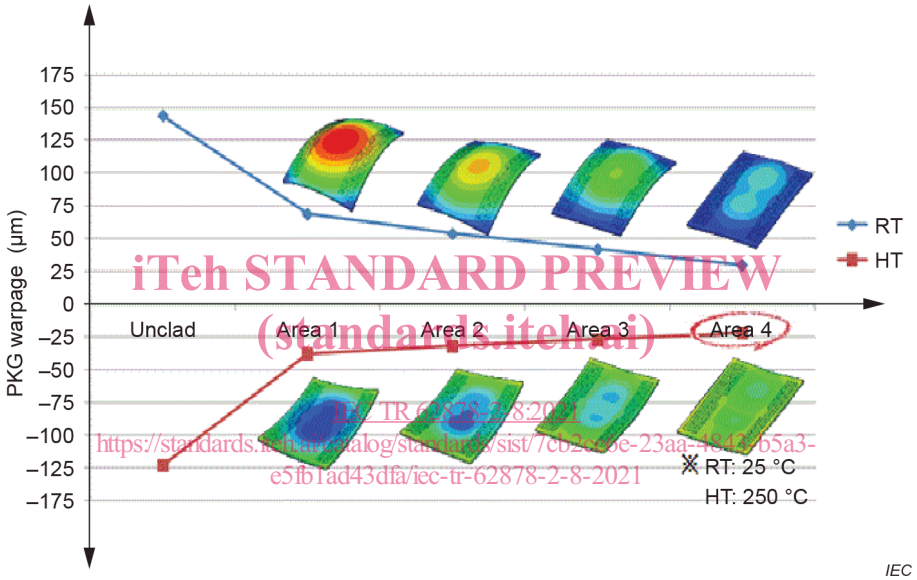
Driving force for Warpage is the CTE mismatch between dielectric materials, circuit layer, embedded device, and solder resistor. While driving force is mainly related to CTE of each layer, the resistance to warpage is heavily dependent on the dimensions of each layer, the height of Si die and the ratio of the die to the panel area. The parameters determining warpage and their relationship are illustrated in Figure 3.

Figure 3 – Parameters determining warpage

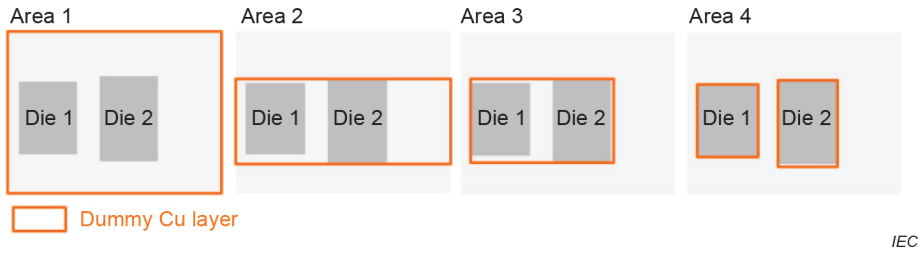
(a) Die embedded substrate without dummy Cu layer



(b) Die embedded substrate with dummy Cu layer



(c) Effects of dummy Cu design on warpage (simulation)



(d) Placements of dummy Cu layer

Figure 4 – Effects of dummy Cu design on warpage

A typical example is included in Figure 4, which shows the CTE mismatch. Without upper Cu layer, the CTE of lower part near dies including multi layers can be much higher than that of the upper part consisting of only thin dielectrics layer because the CTE of die is normally much lower. In that case the neutral axis is shifted to lower direction, which results in the high convex warpage at room temperature and the high concave warpage at high temperature. If the dummy Cu layer is added on the area above the dies, the warpage can be drastically reduced. The greatest reduction in warpage occurs where the dummy Cu layers are confined to the same areas as the die, because the warpage is mainly generated by the CTE difference between Si die and organic substrate