INTERNATIONAL STANDARD

IEC 60748-23-5

QC 165000-5

First edition
2003-10

Semiconductor devices –
Integrated circuits –

Part 23-5:
Hybrid integrated circuits and film structures –
Manufacturing line certification –
Procedure for qualification approval

Dispositifs à semiconducteurs –
Circuits intégrés –

Partie 23-5:
Circuits intégrés hybrides et structures par films –
Certification de la ligne de fabrication –
Procédure d'homologation

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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SEMICONDUCTOR DEVICES – INTEGRATED CIRCUITS –

Part 23-5: Hybrid integrated circuits and film structures – Manufacturing line certification – Procedure for qualification approval

FOREWORD

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International Standard IEC 60748-23-5 has been prepared by subcommittee 47A: Integrated circuits, of IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the European standard EN 165000-5 and the following documents:

FDIS	Report on voting
47A/672/FDIS	47A/677/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

This standard should be read in conjunction with IEC 60748-23-1.

The QC number that appears on the front cover of this publication is the specification number in the IEC Quality Assessment System for Electronic Components (IECQ).

The committee has decided that the contents of this publication will remain unchanged until 2006. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

SEMICONDUCTOR DEVICES – INTEGRATED CIRCUITS –

Part 23-5: Hybrid integrated circuits and film structures – Manufacturing line certification – Procedure for qualification approval

1 Scope

This part of IEC 60748-23 applies to high quality hybrids (with films) incorporating special customer quality and reliability requirements whose quality is assessed on the basis of Qualification Approval.

NOTE 1 Hybrid integrated circuits may be fully or part completed. Part completed devices are those that may be supplied to customers for further processing.

NOTE 2 Test methods are selected from IEC 60748-23-1. A blank detail specification (BDS) is included to assist manufacturers and users in the preparation of detail specifications.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60748-23-1:2002, *Semiconductor devices – Integrated circuits – Part 23-1: Hybrid integrated circuits and film structures – Manufacturing line certification – Generic specification*

IEC 61340-5-1:1998, *Electrostatics – Part 5-1: Protection of electronic devices from electrostatic phenomena – General requirements*

QC 001002-3:1998, *IEC Quality Assessment System for Electronic Components (IECQ) – Rules of Procedure – Part 3: Approval procedures*

3 Terms and definitions

For the purposes of this part of IEC 60748, related documents, preferred ratings and characteristics, and terminology are given in IEC 60748-23-1.

4 Qualification approval procedures

4.1 General

The procedures in QC 001002-3 shall apply.

Subclause 6.1 of IEC 60748-23-1 applies with the exceptions given in 4.2 to 4.11 of this standard.

4.2 Marking

Clause 5 of IEC 60748-23-1 applies.

4.3 Validity of release for delivery

Circuits may be released under qualification approval subject to the following conditions:

a) the circuits conform with the requirements of the detail specification;

b) the circuits, their added components, piece parts and materials are traceable to original manufacturer's lot numbers.

4.4 Application for qualification approval

Application shall be made to the NSI in accordance with QC 001002-3. In addition, the manufacturer shall:

a) conform with the eligibility requirements of 6.1.1 of IEC 60748-23-1;

b) conform with the relevant detail specification based on the blank detail specification (see Clause 6) and the Qualification – product assessment level schedules (Q-PALS) (see Clause 5) contained in this standard.

4.5 Structural similarity

For the purposes of assessment testing, structural similarity can be used if the testing of one representative type of circuit gives at least the same quality level for the rest of the types which are grouped together.

The designated management representative (DMR) shall declare to the satisfaction of the NSI the method of operating the structural similarity plan within the manufacturing facilities and agree the representative type(s) from each structurally similar group.

For the qualification approval procedure, two or more circuits can be considered structurally similar, and thus the required numbers of specimens for a test shall be selected from the combined production, when they have the same function type, use the same design rules, materials, processes and methods (for example a range of T-cell thick film attenuators using the same line of inks; or thin film D/A convertors using the same film material and same added components from the same supplier).

Only those tests not specifically excluded in the Q-PALS may be considered for structural similarity.

4.6 Materials, piece-parts and added components

Subclause 6.1.3 of IEC 60748-23-1 applies.

4.7 Initial qualification approval

The schedules to be used for qualification approval testing on the basis of lot-by-lot and periodic testing are given in the Q-PALS tables contained in this standard.

The procedure for initial qualification approval is given below.

The relevant Q-PALS for initial qualification approval, release of products (lot-by-lot tests) and maintenance of qualification approval (periodic tests) collectively prescribe the minimum test programme on completed circuits.

1) Sampling

   The sample shall be representative of the range of circuits for which approval is sought (see 6.4.3 of IEC 60748-23-1). The size of the sample and the criterion of acceptability depend on the relevant Q-PALS which it is intended to release against.

2) Tests

The complete series of tests specified in the relevant Q-PALS contained in this standard is required for the approval of circuits covered by one detail specification. The tests shall be carried out in the order given.

Test and measurement procedures are given in Clause 7 of IEC 60748-23-1.

Samples used for Group B, C and D tests shall have passed Group A tests.

One failure is counted when a circuit has not satisfied the whole, or a part, of the tests of a group.

Approval is granted when the number of failures does not exceed the specified number of permissible failures for each group or sub-group.

4.8 Granting of qualification approval

The manufacturer shall submit a report to the NSI covering the qualification approval testing in accordance with the requirements of 4.7 of this standard, and with QC 001002-3.

Qualification approval shall be granted when the requirements of this standard have been satisfied.

A qualification approval certificate will be issued by the responsible national authority in accordance with QC 001002-3.

4.9 Maintenance of qualification approval

4.9.1 General

Qualification approval is maintained after successful completion of the procedures and requirements of quality conformance inspection (see 6.4.2 of IEC 60748-23-1) with the following details:

1) Design evaluation tests

In addition to the initial delivery lot, design evaluation tests shall be carried out at the periodicity specified in the detail specification.

2) Detail specification

The detail specification shall conform to the requirements of the BDS and Q-PALS in this standard.

The manufacturer shall also have maintained continuous production, for example:

a) no change has occurred in the place of manufacture and final test;

b) no break exceeding two years has occurred in the manufacturer's declared periodic test schedule.

4.9.2 Changes to qualification approval

The manufacturer is required to notify the NSI of changes to his qualification approval in accordance with QC 001002-3 and 6.5.2 of IEC 60748-23-1, where applicable.

NOTE All re-verification programmes are to be agreed with the NSI.

4.10 Procedure in the event of a failure in a periodic test

The procedure described in QC 001002-3 shall apply.

4.11 Withdrawal of qualification approval

The procedures in QC 001002-3 shall apply.

5 Qualification-product assessment level schedules

NOTE The following 11 Q-PALS are based upon corresponding PALS in IEC 60748-23-1, Annex A.

Q-PRODUCT ASSESSMENT LEVEL SCHEDULE 1

Applicability

This assessment schedule is intended for use with solder assembled and/or bare die, non-hermetic encapsulated, unencapsulated, cavity or non-cavity devices, which are for use in benign mechanical and temperature environments.

Subgroup A tests: Device screening 100 %	**IEC 60748-23-1 Reference**
1. Electrical test at T_{amb}. Those tests in the detail specification which define circuit functionality	7.4

Subgroup B tests (lot-by-lot): Device sample testing – IL S4 AQL 0,4 %

1. Electrical test at T_{amb} (other than those specified for screening)	7.4
2. External visual inspections	7.3.2

Subgroup C tests (6 monthly period): Design evaluation

Minimum sample 8. Accept on 0 failures.

1. Electrical test. All specified parameters at T_{min} and T_{max}*	7.4
2. Dimensions	7.3.3

Subgroup D tests (12 monthly period): Design evaluation

Minimum sample 3. Accept on 0 failures.

1. Resistance of circuits to solder heat	(D)	7.5.11
2. Solderability	(ND/D)	7.5.10
3. Robustness of terminations	(D)	7.5.12
4. Flammability	(D)	7.5.16
5. Resistance to solvents	(ND)	7.5.15

Process and packaging requirements

1. Substrate fabrication = class 100 000.
2. Substrate assembly (bare die) = class 100 000.
3. ESD precautions (where applicable) to IEC 61340-5-1.
4. Pre-cap visual at IL S4 AQL 0,4 % minimum. 7.3.1

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* Structural similarity rules do not apply.

Q-PRODUCT ASSESSMENT LEVEL SCHEDULE 2

Applicability

This assessment schedule is intended for use with solder assembled and/or bare die, non-hermetic encapsulated, unencapsulated, cavity or non-cavity devices, which are for use in benign mechanical and temperature environments.

Subgroup A tests: Device screening 100 %	**IEC 60748-23-1 Reference**
1. Electrical test at T_{amb}. Those tests in the detail specification which define circuit functionality	7.4

Subgroup B tests (lot-by-lot): Device sample testing – IL S4 AQL 0,4 %

1.	Electrical test at T_{amb} (other than those specified for screening)	7.4
2.	External visual inspection	7.3.2

Subgroup C tests (6 monthly period): Design evaluation

Minimum sample 8. Accept on 0 failures

1.	Electrical endurance 1 000 h. Release after 160 h*	7.5.14
2.	Electrical test. All specified parameters at T_{min} and T_{max}*	7.4
3.	Dimensions	7.3.3

Subgroup D tests (12 monthly period): Design evaluation

Minimum sample 3. Accept on 0 failures

1.	Resistance of circuits to solder heat	(D)	7.5.11
2.	Solderability	(ND/D)	7.5.10
3.	Robustness of terminations	(D)	7.5.12
4.	Flammability	(D)	7.5.16
5.	Resistance to solvents	(ND)	7.5.15

Process and packaging requirements

1.	Substrate fabrication = class 100 000.	
2.	Substrate assembly (bare die) = class 100 000.	
3.	ESD precautions (where applicable) to IEC 61340-5-1.	
4.	Pre-cap visual at IL S4 AQL 0,4 % minimum.	7.3.1

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* Structural similarity rules do not apply.