IEC 61188-6-3

Edition 1.0 2024-12

INTERNATIONAL STANDARD

NORME INTERNATIONALE

colour inside

Circuit boards and circuit board assemblies – Design and use – Part 6-3: Land pattern design – Description of land pattern for through hole components (THT)

Cartes imprimées et cartes imprimées équipées – Conception et utilisation – Partie 6-3: Conception de la zone de report – Description de la zone de report pour les composants à trous traversants (THT)

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IEC 61188-6-3 has been prepared by IEC technical committee 91: Electronics assembly technology. It is an International Standard.

This first edition partially cancels and replaces the IEC 61188-5 series of International Standards.

The significant technical changes with respect to the previous edition are listed in the Introduction and further detailed information and calculations can be found in Annex A.

The text of this International Standard is based on the following documents:

Draft	Report on voting
91/1982/FDIS	91/1997/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

A list of all parts in the IEC 61188 series, published under the general title *Circuit boards and circuit board assemblies – Design and use*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

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INTRODUCTION

The new series IEC 61188-6-xx replaces the below listed documents:

IEC 61188-5-1:2002, *Printed boards and printed board assemblies – Design and use – Part 5-1: Attachment (land/joint) considerations – Generic requirements*

IEC 61188-5-2:2003, *Printed boards and printed board assemblies – Design and use – Part 5-2: Attachment (land/joint) considerations – Discrete components*

IEC 61188-5-3:2007, *Printed boards and printed board assemblies – Design and use – Part 5-3: Attachment (land/joint) considerations – Components with gull-wing leads on two sides*

IEC 61188-5-4:2007, *Printed boards and printed board assemblies – Design and use – Part 5-4: Attachment (land/joint) considerations – Components with J leads on two sides*

IEC 61188-5-5:2007, *Printed boards and printed board assemblies – Design and use – Part 5-5: Attachment (land/joint) considerations – Components with gull-wing leads on four sides*

IEC 61188-5-6:2003, *Printed boards and printed board assemblies – Design and use – Part 5-6: Attachment (land/joint) considerations – Chip carriers with J-leads on four sides*

IEC 61188-5-8:2007, *Printed boards and printed board assemblies – Design and use – Part 5-8: Attachment (land/joint) considerations – Area array components (BGA, FBGA, CGA, LGA)*

The content of the above documents is based on IPC-SM-782 Rev. A with Amendments 1 and 2, which was replaced in 2002 by IPC-7351. The component spectrum and pitch levels have dramatically changed since publication of the 61188-5-xx series and its dimensioning concept no longer fulfils state of the art mounting and soldering requirements.

This document provides guidelines and focus on land pattern for through hole terminals (THT).

Within the previous standards, primarily the pin diameter of the component and the assembly tolerances were considered.

The new approach is that a sufficiently available (proportional) land pattern is related to:

- size and shape of the component terminal
- the requirements of the assembly process and its used tools
- technology, structure, thickness and manufacturing process of the circuit board

in order to achieve the best possible solder joint due to manufacturability, the assembly result and the reliability of an assembled circuit board.

The variety and the possibility of building printed circuit boards has grown considerably over the years. The technologies can become very complex. The proportion of copper in the circuit board is determined by the number of layers or copper thickness per layer. This could lead to higher thermal capacity of the circuit board.

The general use of soldered THT components has declined dramatically. The requirements for current carrying capacity (e.g. wire thickness of inductors) have increased for the through-hole components used. At the same time, the use of wave soldering has declined in favour of selective wave soldering or other technologies.

A balance between heat source (soldering process) and heat sink (component or component pin and circuit board) must be found for required assembly results. The landing surface must be defined according to these requirements.

Detailed information and calculations can be found in Annex A.

CIRCUIT BOARDS AND CIRCUIT BOARD ASSEMBLIES – DESIGN AND USE –

Part 6-3: Land pattern design – Description of land pattern for through hole components (THT)

1 Scope

This part of IEC 61188 specifies the requirements for lands and land pattern on circuit boards for the mounting of components with leads by soldering based on the solder joint requirements of IEC 61191-1 and IEC 61191-3.

This part of IEC 61188 specifies the requirements for soldering surfaces on circuit boards. This includes lands and land pattern for surface mounted components and also solderable hole configurations for through hole mounted components. These requirements are based on the solder joint requirements of IEC 61191-1, IEC 61191-2, IEC 61191-3 and IEC 61191-4.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60194-2, *Printed boards design, manufacture and assembly – Vocabulary – Part 2: Common usage in electronic technologies as well as printed board and electronic assembly technologies*

IEC 60352-5:2020, *Solderless connections – Part 5: Press-in connections – General requirements, test methods and practical guidance*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60194-2 and the following apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

- IEC Electropedia: available at https://www.electropedia.org/
- ISO Online browsing platform: available at https://www.iso.org/obp

3.1
annular ring
amount of land that remains after a hole is drilled in the defined Padstack

3.2
finished hole size (FSH)
diameter after all metallization processes (galvanic processing) and additional surface finishing processes (final finish) have been completed

3.3
solder source side
side which is in contact with solder material (e.g. soldering wave, solder tip), usually the opposite side of the assembled THT component

3.4
solder target side
side where the component is usually placed

Note 1 to entry: The solder material will fill the THT from the opposite side (solder source side).

4 Description of a through hole component

4.1 Component body

Leaded components consist of a so-called body with electrical functional elements and leads which enable the connection to the circuitry of the circuit board by soldering (see Figure 1).

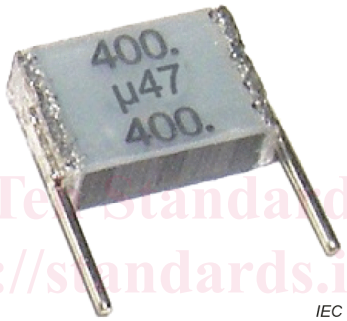

Figure 1 – Leaded component

4.2 Component leads

Leads of components for through hole mounting usually have a round, square or rectangular profile. For the Padstack design the maximum diameter of the lead is the determining parameter. The diameter of the through hole depends on the shape of the lead (for typical variations of leads see Figure 2, Figure 3 and Figure 4).

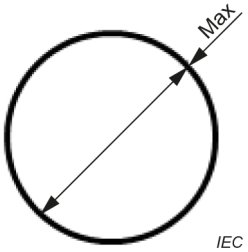

Figure 2 – Round lead

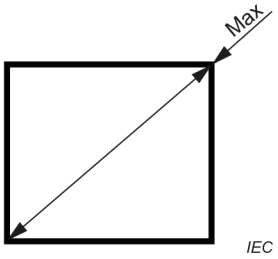

Figure 3 – Square lead

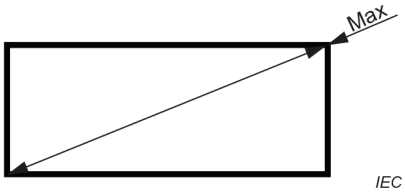

Figure 4 – Rectangle lead

5 Padstack

5.1 Description

A Padstack is the definition of the size and shape of the pads on each of the layers of a circuit board plus the definition of the hole size and type. Form and size of the pad depends on the lead form and size and the component body.

5.2 Pad types

5.2.1 General

There are specific functions using different shapes on different layer. Within the Library, a Padstack shall be described in general with all optional functions.

5.2.2 General

Depending on the layer function in the circuit board layer stack the pad function also will be different. Table 1 and Figure 5 give an overview of the relation between layer functionality and associated pad type.

Table 1 – Layer function and pad types

Layer function	Pad type	display
Solder mask	Top and bottom solder mask	negative data
Outer layer	Top and bottom pad (Land)	positive data
Inner signal layer	Inner layer pad	positive data
Inner power layer	Plane thermal or plane anti-pad	negative data

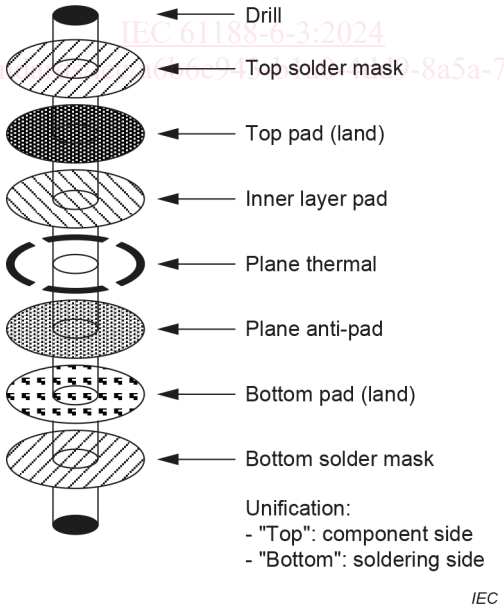

Figure 5 – Padstack

5.2.3 Solder mask pads

The solder mask pads define the metallic surface of the solder joint. Within the CAD tool the solder mask is displayed as inverse.

5.2.4 Outer layer pads

Outer layer pads describe the copper area which fixes the soldered device with the outer layer. Sometimes it can be helpful to distinguish between the component and the solder side.

5.2.5 Thermal pads

The feature of a thermal pad is used to prohibit heat dissipation during the soldering process, to get a reliable solder joint without degrading the circuit board base material.

5.2.6 Anti-pads

The so-called anti-pads are used to ensure insulation between the inner layer copper pads and the copper area of power planes. Usually the minimum size of the anti-pad is the minimum isolation distance of copper elements with different nets and the size of the inner layer pad.

5.3 Pad shapes

The basic elements of the Padstacks are polygons on each layer which represent the copper structures of the circuit board. These polygons can be circular, square or rectangular with rounded or chamfered corners or even variations of this shapes.

Sometimes a special pad shape such as a square pad on the component layer of the circuit board is used as pin 1 indicator.

5.4 Holes – Considerations for plated-through hole dimensioning

The used assembly technique will influence the hole diameter, additionally the number of pins per device and their alignment. Different assembly techniques shall have different hole calculations:

- The way of creating the hole (drilling, milling, punching, additive manufacturing, others)
- Insertion during assembly process (manual or automatic)
- Soldering process (manual, automatic, wave soldering, Through-Hole Reflow, others)
- Press fit terminals (Press in)

For the tolerance analysis, the dimensions considered for the lead to hole relationship come with an assumption that the end product hole diameter is a plated-through hole. Thus, the drilled hole diameter is somewhat larger in order to fulfil the requirements for the plating thickness of the hole wall.

Regarding multilayer internal Padstack requirements, the sum of the drillbit diameter and the minimal necessary annular ring determines the pad size and thus the relationship between the land and lead diameter have been compensated by adding 0,1 mm to the hole clearance requirement in order to accommodate the plating of the through-hole.

The land size (land shape) therefore considers all the features that make up the land to hole relationship. Usually the through-hole land requirements are based on multilayer technology. If a single side circuit board is used, the hole size must be a little bigger. However, since the requirements for attachment require a lead clinch, the concepts used in this document can work for both plated and non-plated hole characteristics.

In the event that a non-plated hole is used to attach a component lead, which cannot be bent, the clearance between the lead and the hole is critical in order to reduce the amount of excess room for the solder attachment. In this instance the hole to lead relationship is reduced to a minimum clearance of 0,015 mm between the hole diameter and the maximum lead diameter. The land pattern concepts provided in this document shall have the hole size reduced, however it is recommended that the original land size be maintained in order to provide for a reliable solder joint formation.

Within the solderless connection of Press-in terminals, the diameter of the drilled hole is defined in the manufacturer's datasheet or applicable standards (IEC, IPC).

The land pattern of THT devices used on very thin rigid substrates, foil, flexible, or stretchable materials will have a different shape compared to typical rigid Substrates. Some devices use solderable mechanical snap-in pins e.g. to adopt the connector-Plug-in forces. For those holes the finished hole size diameter is usually described in the specification of the device. If the through-hole has additional functions, which are not described within this document, the land pattern design has to be aligned between supplier, designer (librarian), circuit board manufacturer and electronic manufacturing service.

5.5 Annular ring

An annular ring is defined as the amount of land that remains after a hole is drilled through it. Depending on the size of the annular ring a more or less robust solder joint will be formed. Therefore it may be a good choice to work with a proportional concept also for the relation between lead diameter and annular ring.

The size of the annular ring of press-in connections shall meet the requirements of the manufacturer's database and IEC 60352-5.

6 Requirements on lands for solder joints

6.1 General

The calculation of a land pattern is based on the component terminal diameter (see Figure 6). Figure 7 shows the basic design flow diagram for land pattern for THT.

As a result of proper land and hole dimensioning a reliable solder joint will be formed during the soldering process. Thus, it is necessary to know which soldering method will be used during the manufacturing of the circuit board assembly.