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Device embedding assembly technology –
Part 2-603: Guideline for stacked electronic module – Test method of intra-module electrical connectivity

Techniques d'assemblage avec appareil(s) intégré(s) –
Partie 2-603: Lignes directrices pour un empilement de modules électroniques – Méthode d'essai de la connectivité électrique entre modules

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DEVICE EMBEDDING ASSEMBLY TECHNOLOGY –

**Part 2-603: Guideline for stacked electronic module –
Test method of intra-module electrical connectivity**

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IEC 62878-2-603 has been prepared by IEC technical committee 91: Electronics assembly technology. It is an International Standard.

The text of this International Standard is based on the following documents:

Draft	Report on voting
91/1999/FDIS	91/2016/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

A list of all parts in the IEC 62878 series, published under the general title *Device embedding assembly technology*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

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INTRODUCTION

High-end servers, network systems, PCs and smart phones have been driving the electronic assembly technologies for the last couple of decades. In order to meet higher demands in computing load from cloud computing and large scale of datacentres with low energy consumption and cost-effective manner, it is important that IoT and edge computing devices achieve greater miniaturization and densification. Stacked electronic module which offers complex and simultaneous integration of various functional modules and specific features is a solution that can meet these demands. The stacked electronic module is produced by means of stacking some stackable electronic modules. The stackable electronic module usually mounts components with area array type package (BGA, LGA, and similar) on the surface and does embed components with wafer-level type package or bare chip into the inner layer to achieve miniaturization and densification. However, from a viewpoint of test and diagnosis the stacked electronic module becomes an invisible, untouchable and undiagnosed structure. Due to its design and construction complexity, it is increasingly critical to test a stacked electronic module with a combination of conventional methods such as external input/output (I/O) terminal or in-circuit test with advanced methods (e.g. boundary scan or bi-directional bus control).

This document is one of a series of guidelines for stacked electronic modules.

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DEVICE EMBEDDING ASSEMBLY TECHNOLOGY –

Part 2-603: Guideline for stacked electronic module – Test method of intra-module electrical connectivity

1 Scope

This part of IEC 62878 specifies the electrical test method to detect electrical connectivity defects of the stacked electronic module caused by the stacking assembly process to stack some stackable electronic modules. This method is realized to make use of bidirectional serial communication bus interface applied to the stackable electronic modules which are assured as "known good module" (KGM).

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

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IEC 60194-2, *Printed boards design, manufacture and assembly – Vocabulary – Part 2: Common usage in electronic technologies as well as printed board and electronic assembly technologies*

3 Terms, definitions and abbreviated terms

3.1 Terms definitions

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For the purposes of this document, the terms and definitions given in IEC 60194-2 and the following apply.

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3.1.1
known good module
KGM
electronic module, which meets quality, reliability, performance and functionality as agreed upon between customer and supplier

3.2 Abbreviated terms

SAEM stackable electronic module

SDEM stacked electronic module

4 General

The SDEM is produced by means of stacking at least more than two stackable electronic modules. The SAEM usually mounts components with area array type package on the surface and does embed components with wafer-level type package or bare chip into the inner layer to achieve miniaturization and densification. Figure 1 depicts a SAEM. Figure 2 depicts a SDEM to stack three SAEMs.

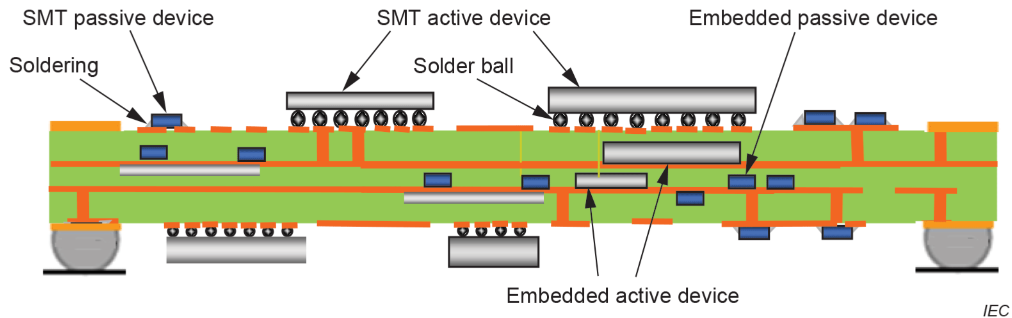

Figure 1 – SAEM (stackable electronic module)

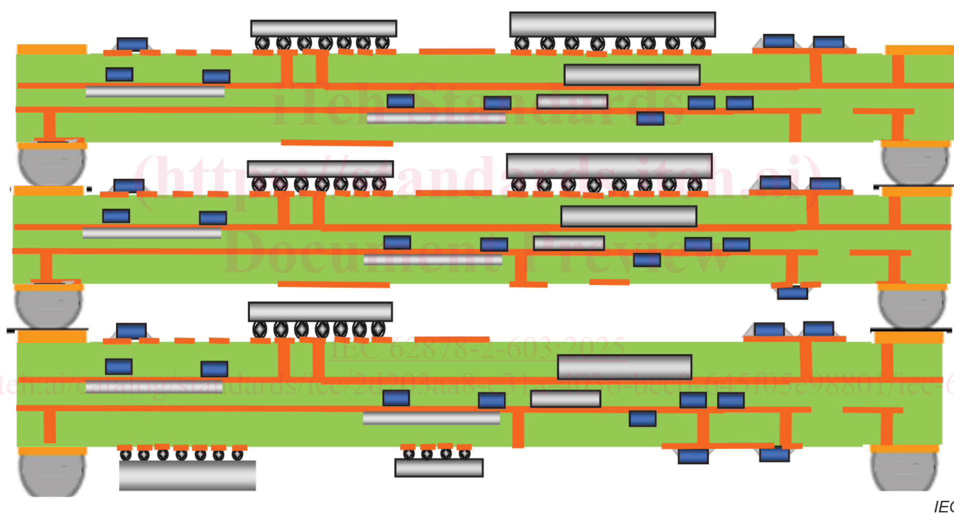

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Figure 2 – SDEM (stacked electronic module)

The SDEM is produced by means of stacking some SAEMs which should be KGM to meet quality, reliability, performance and functionality as agreed upon between user and supplier.

a) KGM shall be individually tested before assembly.

b) Intra-module connections of SAEMs shall be tested before stacking assembly.

c) After stacking assembly the inter-module connections of SDEM shall be tested.

Figure 3 shows inter-module connection and intra-module connection.

If a SDEM is produced by use of pre-tested SAEMs, it is sufficient to test the electrical connections between the individual SAEMs for the purpose of assuring the functionality of the SDEM.

In Clause 5 to Clause 7, an example is described, how this test strategy can be realized by utilization of the bidirectional I2C (Inter-Integrated Circuit) bus.

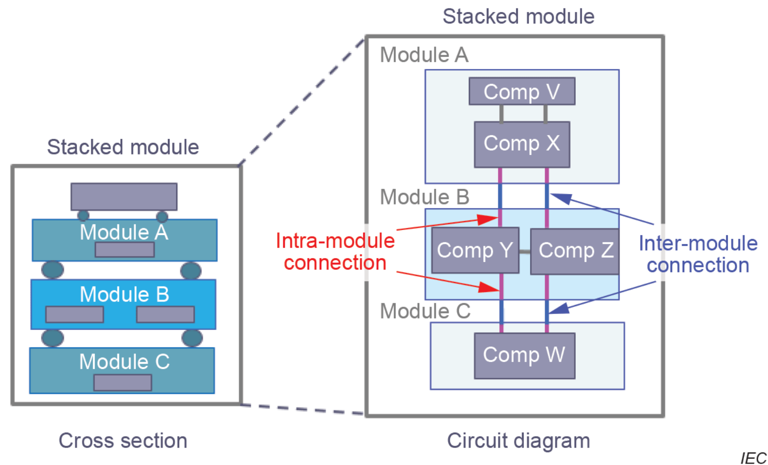

Figure 3 – Inter-module connection and intra-module connection

The external appearance test and the open or short test should be generally performed as precondition of any electrical tests before the electrical connectivity test, so that any breakdown should be prevented when power is supplied. The external appearance test should detect misorientation and misalignment between SAEMs. Also, the open or short test should detect open circuit and short circuit between power supply line and ground line.

Various test methods on external appearance test and the open or short test are developed and widely applied respectively. Since it is so difficult to standardize them, they should be out of the scope of this document.

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5 Test specimen

5.1 General

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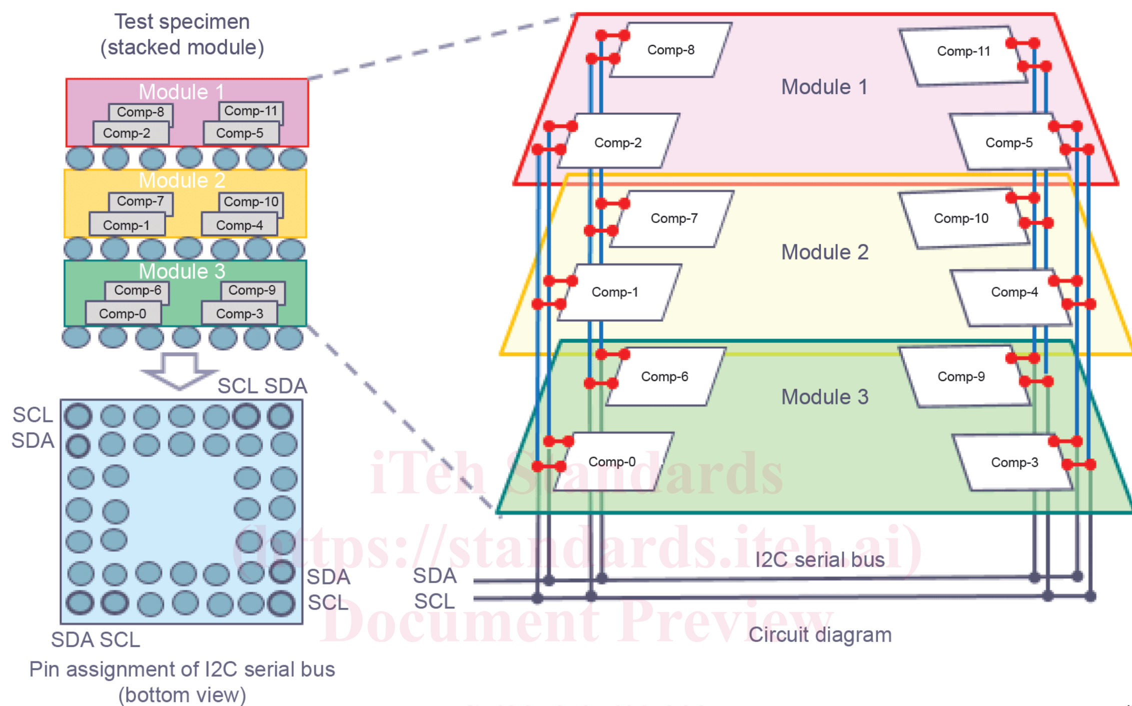
Since the SDEM becomes an invisible, untouchable and undiagnosed structure from a viewpoint of test and diagnosis, it is required to make use of bidirectional serial communication bus interface applied to the SAEMs which are assured as KGM. Some bidirectional serial communication bus interfaces are well-known and in reality, have been applied to actual electronic products. Three representatives such as I2C, Joint Test Action Group Boundary-Scan and SPI to mutually connect among electronic components are shown in Annex A. The test specimen adopt I2C of a simple 2-wire serial communication interface to achieve miniaturization, densification and to consider test design cost and accessibility of electronic components in the marketplace as well. It also adopts lead-free solder joint method as a stacking assembly method. Annex A shows representative examples of stacking assembly methods described in IEC 62878-2-602:2021).

5.2 Preparation of test specimen

The test specimen is a SDEM which is produced by means of stacking at least more than two SAEMs. Each of SAEMs should have some embedded components which are compliant with I2C serial communication bus interface protocol. The components should have two dedicated terminals such as SDA and SCL and do their own unique number to be distinguished from others. The two bus lines such as SDA and SCL are connected to the two dedicated terminals of every embedded component of the stacked module and to a test apparatus as well.

Figure 4 shows an image drawing of the test specimen which consists of the cross section of the test specimen, the circuit diagram and the bottom view. This example stacks three SAEMs such as Module 1, Module 2 and Module 3. Each SAEM has at least four embedded components. That is, Module 1 has Comp-2, Comp-5, Comp-8 and Comp-11. Module 2 has Comp-1, Comp-4, Comp-7 and Comp-10. Module 3 has Comp-0, Comp-3, Comp-6 and Comp-9. The other components can be embedded and/or mounted in order to evaluate embedding assembly process although they are not explicitly shown in the Figure 4. In this example, there are forty external terminals and eight ones of them are assigned to I2C serial communication bus lines such as SDA and SCL near four corner sides.



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NOTE Blue line shows inter-module connection and red line shows intra-module connection.

Figure 4 – Image drawing of the test specimen

6 Test apparatus

The test apparatus consists of a base board, a controller and a converter box. The base board mounts a test specimen and connect to the test specimen and the controller through bidirectional serial communication bus. the controller manages bidirectional serial communication bus and has test program software to test electrical connectivity of the test specimen. Finally, the converter box bi-directionally converts between USB and other serial communication buses.

Figure 5 shows test apparatus to choose I2C as a serial communication bus interface.