IEC 63373

Edition 1.0 2022-02

INTERNATIONAL STANDARD

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Dynamic on-resistance test method guidelines for GaN HEMT based power conversion devices

Lignes directrices pour les méthodes d'essai de résistance dynamique à l'état passant des dispositifs de conversion de puissance fondés sur les HEMT en GaN

IEC 63373:2022-02(en-fr)

IEC Secretariat
3, rue de Varembé
CH-1211 Geneva 20
Switzerland

Tel.: +41 22 919 02 11
info@iec.ch
www.iec.ch

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

COMMISSION ELECTROTECHNIQUE INTERNATIONALE

ICS 31.080.99

ISBN 978-2-8322-1076-6

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DYNAMIC ON-RESISTANCE TEST METHOD GUIDELINES FOR GaN HEMT BASED POWER CONVERSION DEVICES

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Draft	Report on voting
47/2690/CDV	47/2735/RVC

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The language used for the development of this International Standard is English.

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[1] Numbers in square brackets refer to the Bibliography.

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INTRODUCTION

This document is intended for use in the GaN power semiconductor and related power electronic industries, and provides guidelines for measuring the dynamic ON-resistance of GaN power devices.

Gallium Nitride (GaN) lateral power High Electron Mobility Transistor (HEMT) conducts through a two-dimensional electron gas (2DEG) in ON-state operation. Due to the various stress conditions that the device encounters during power electronic switching applications, some charge could get trapped in specific regions of the transistor structure. The trapped electrons cause an increased ON-resistance when operated in a switching environment. This phenomenon is known as current collapse and the ON-resistance at switching operation is called dynamic ON-resistance in order to distinguish from DC ON-resistance. Increased dynamic ON-resistance translates to higher power loss, thereby reducing overall system efficiency. Not verifying the dynamic ON-resistance characteristic can put GaN device reliability at risk [2].

The test methods provided in this document can be used as a guideline for measuring dynamic ON-resistance of GaN power device, focused on lateral HEMT technologies. These three test methods can be applied for datasheet, process control, technology development, final tests and other usage. Parasitic effects impact high precision measurements and wafer level tests can minimize parasitic effects. Additionally, self-heating can impact the package level tests depending upon the package thermal characteristics.

DYNAMIC ON-RESISTANCE TEST METHOD GUIDELINES FOR GaN HEMT BASED POWER CONVERSION DEVICES

1 Scope

In general, dynamic ON-resistance testing is a measure of charge trapping phenomena in GaN power transistors. This publication provides guidelines for testing dynamic ON-resistance of GaN lateral power transistor solutions. The test methods can be applied to the following:

a) GaN enhancement and depletion-mode discrete power devices [3];

b) GaN integrated power solutions;

c) the above in wafer and package levels.

The prescribed test methods can be used for device characterization, production testing, reliability evaluations and application assessments of GaN power conversion devices. This document is not intended to cover the underlying mechanisms of dynamic ON-resistance and its symbolic representation for product specifications.

2 Normative references

There are no normative references in this document.

3 Terms, definitions, symbols and abbreviated terms

3.1 Terms and definitions

No terms and definitions are listed in this document.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.2 Symbols and abbreviated terms

Symbol or abbreviation	Name or term
DUT	Device Under Test
V_{DD}	Supply voltage
V_{DS}	Drain to Source Voltage of DUT
V_{GS}	Gate to Source Voltage of DUT
D1	Free-wheeling diode
L	Inductance
R	Resistance
C	Capacitance
I_D	Drain current of DUT in ON-state
$V_{DS(ON)}$	Drain to Source Voltage of DUT in ON-state
$R_{DS(ON)}$	Drain to Source Resistance of DUT in ON-state

Symbol or abbreviation	Name or term
$V_{DS(OFF)}$	Drain to source voltage of DUT in OFF-state
$V_{GS(ON)}$	Gate to source voltage of DUT in ON-state
$V_{GS(OFF)}$	Gate to source voltage of DUT in OFF-state
t_{off}	OFF-state pulse width
t_{on}	ON-state pulse width
$t_{m,on}$	measurement timing in ON-pulse
t_{dn}	Soft-switching delay time between the OFF and ON pulse or vice-versa, with n = 1 or 2
f	Frequency
N	Number of pulses
T_C	Case temperature
P_{Peak}	Instantaneous peak power, applicable for only hard switching
E_{Pulse}	Energy dissipated per pulse, applicable for only hard switching

4 Test circuits and waveforms

4.1 General

GaN power transistors typically are being targeted for both hard and soft-switching topologies for power conversion applications.

Hard switching conditions refer to the overlap of the voltage and current waveforms when the power device switches either from ON-to-OFF or OFF-to-ON states. Typical hard-switching topologies include totem-pole Power Factor Correction (PFC) boost converters, buck converters, motor control inverter and single ended fly-back circuits.

Soft switching conditions refer to conditions where there is no or minimal overlap of the voltage and current waveforms when the GaN power device switches between the ON- and OFF-states. Typical soft-switching topologies include Zero Voltage Switching (ZVS) converters, LLC converters, Active Clamp Fly-back (ACF), etc.

Resistive load switching is another type that is not typically seen in the power electronic applications whose overlap of voltage and current waveforms fall in between the hard and soft switching types. However, the easier implementation of this switching type makes it attractive for the device level characterization and testing purposes.

As described above, current-voltage loci are the crux that determines the switching type. The loci of above three switching types are explained with great detail in here [4]. The following 4.2 and 4.3 cover the dynamic ON-resistance measurement methods for these three switching types.

Minimizing parasitic effects when performing high precision measurements is recommended. Wafer level tests can be used to minimize parasitic effects when performing high precision measurements. For package level tests, the impact of package thermal characteristics should be considered so as to minimize any device under test (DUT) self-heating implications.

4.2 Inductive and resistive switching methods

A hard-switching inductive and resistive loaded test vehicle that is analogous to what is generally termed the “double-pulse” tester in power electronic applications [2] is shown in

Figure 1. Another depiction of the double-pulse tester is shown in Figure 2, which illustrates that the double-pulse tester is equivalent to a boost converter with the input tied to the output [5]; note that R_{Load} = 0 in this depiction.

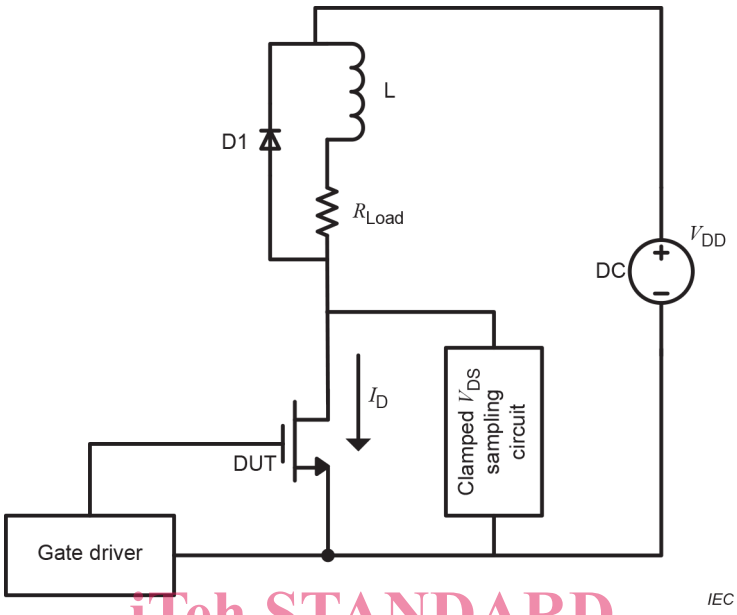

Figure 1 – Inductive-resistive load "double-pulse" test circuit for hard-switching evaluation

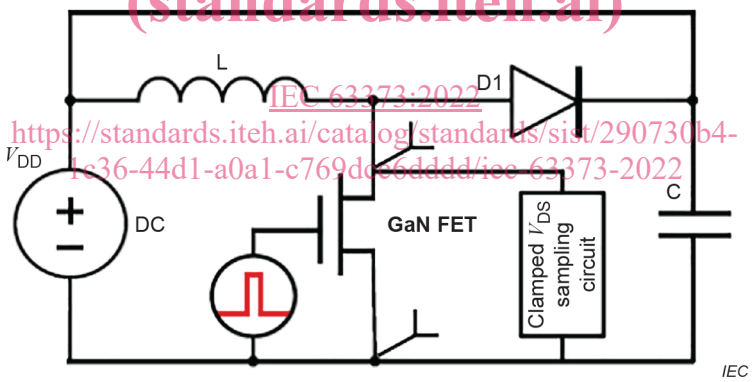

Figure 2 – Depiction of the hard-switching "double-pulse" test circuit (showing its similarity to a boost converter)

When a power transistor switches at high voltages, measuring the drain-to-source ON-state voltage with a passive probe in combination with an oscilloscope can be quite challenging, as the oscilloscope's dynamic-range precision may not be adequate. As an example, consider a device with an ON-state voltage of 0,5 V at 1 A of drain current switching from 400 V in the OFF-state. An 8-bit oscilloscope configured to measure the 400 V OFF-state voltage will have a resolution of 1,562 5 V (= $400/2^8$), which is not sufficient to measure the 0,5 V ON-state voltage. The measurable voltage has an error of more than 3 times the actual voltage in this example and this further increase to 30 times to detect a 10 % dynamic ON-state voltage drift. To circumvent such problems, a circuit may be employed to clamp the high OFF-state voltage on a low-voltage measurement probe without compromising the ON-state voltage.

Since the clamped sampling circuit reduces the voltage swing quite significantly on the measurement probe, the dynamic ON-state voltage of the power transistor can be effectively measured, from which its dynamic ON-resistance is calculated using Ohm's law. Some examples of voltage clamp sampling circuits are reported in [6] and [7].

It is to be noted that if R_{Load} = 0 in Figure 1 (which makes the circuits of Figure 1 and Figure 2 identical), the circuit is nothing but a standard power electronics double-pulse or boost test circuit. The hard-switching circuits presented in Figure 1 and Figure 2 provide the flexibility of running tests either in single-pulse, double-pulse or continuous-pulse modes. They provide high impedance on the drain, which lowers V_{DS} without the need for an additional synchronized tester resource. A high impedance may also be achieved by setting L = 0 and using a high-value resistor making this a pure resistive switching. The single and double-pulse test modes are often advantageous in production environments where fast switching characterization is needed, whereas the continuous-pulse test mode is beneficial for longer-term device characterization and reliability evaluation. The flow chart for inductive and/or resistive switching load-based measurement is presented in Figure 3, and Figure 4 shows the representative hard-switching waveforms of a GaN power transistor in the Figure 1 and Figure 2 test circuits when subjected to continuous gate pulses. In a pure resistive switching load test circuit, the DUT current in ON-state stays constant unlike the inductive load circuit where the current increases linearly with time. A high-performance clamp circuit design may be required to measure the drain-to-source dynamic ON-resistance in <1 µs after the device transitions from the OFF-state to the ON-state. The $R_{DS(ON)}$ is evaluated dynamically during the period when the transistor gate is ON as $R_{DS(ON)} = V_{DS(ON)}/I_D$.

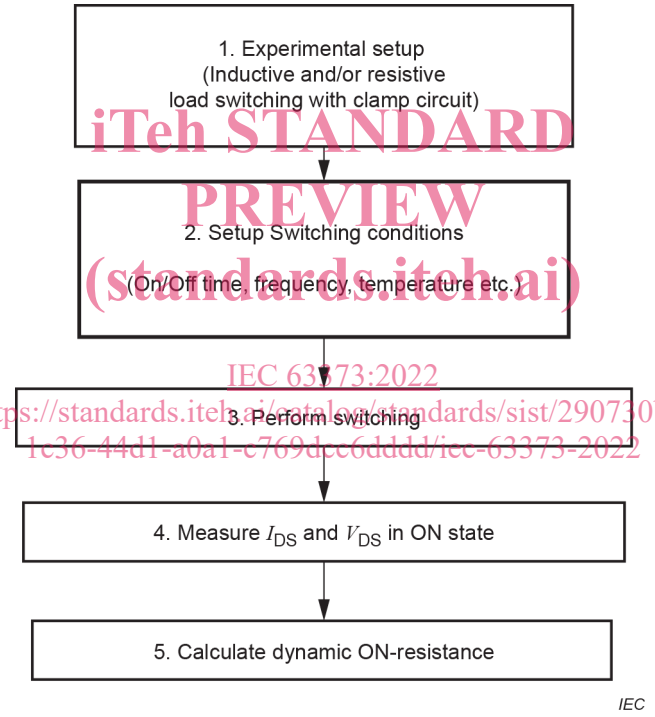

Figure 3 – Simplified flowchart for inductive and/or resistive switching based dynamic on-resistance test

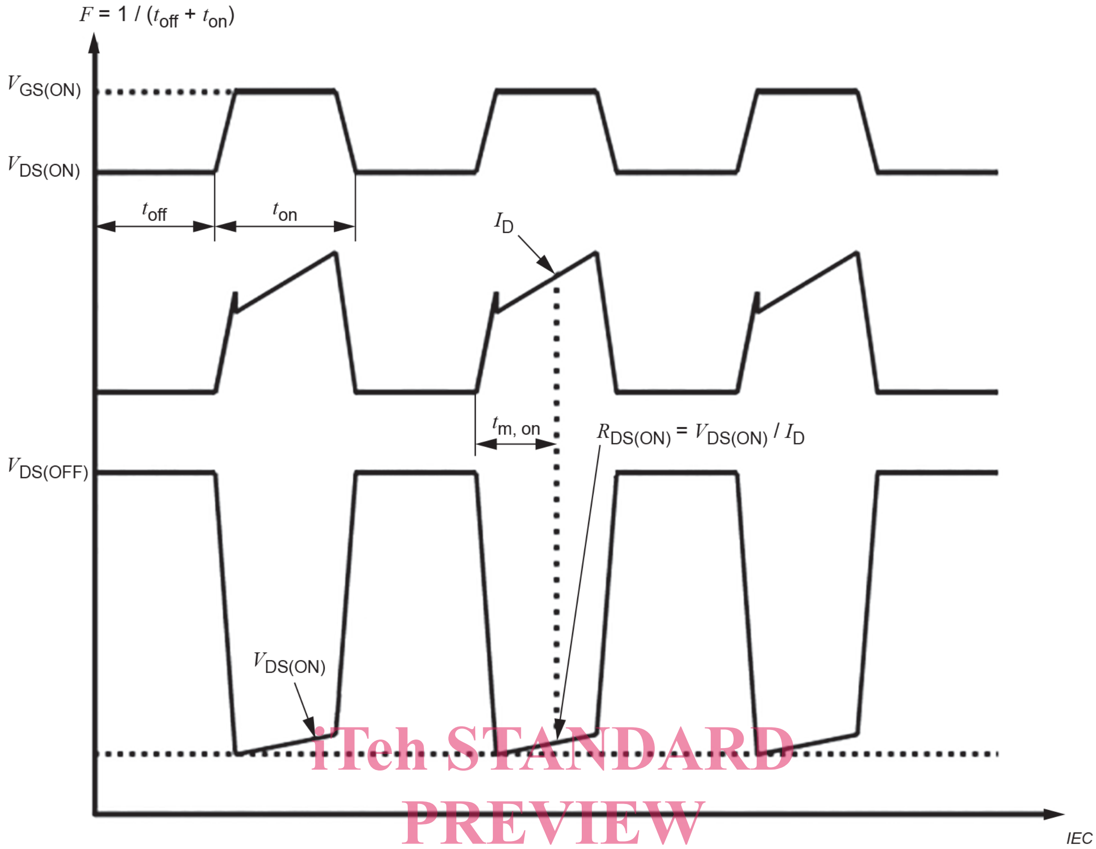

Figure 4 – Representative continuous-pulse hard-switching waveforms for measuring dynamic on-resistance using the test circuits in Figure 1 and Figure 2

4.3 Pulsed current-voltage (I-V) method

The pulsed I-V technique is analogous to soft switching, which is widely used in GaN RF electronics. This method involves pulsing the gate and drain voltage signals independently, and hence is branded as a classic "double pulse" technique in the RF world, thus potentially leading to confusion since this term is used in the power electronics world to refer to a hard-switching test, as discussed above. Using this approach, a few manufacturers have developed systems to fulfil power electronic requirements [8]. Figure 5 and Figure 6 provide simplified test setup and test flow respectively for soft switching.

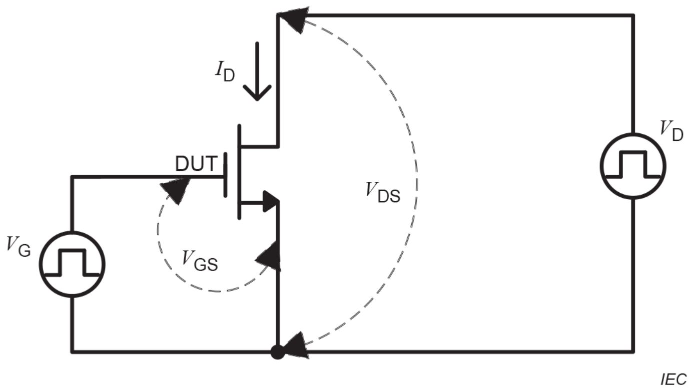

Figure 5 – Example test circuit for soft-switching on-resistance measurement (the gate and drain terminals are pulsed with independent voltage signals)