IEC 62530-2

Edition 1.0 2021-07

INTERNATIONAL STANDARD

IEEE Std 1800.2™

SystemVerilog –
Part 2: Universal Verification Methodology Language Reference Manual

IEC 62530-2:2021-07(en) IEEE Std 1800.2-2017

IEC Central Office
3, rue de Varembé
CH-1211 Geneva 20
Switzerland
Tel.: +41 22 919 02 11
info@iec.ch
www.iec.ch

Institute of Electrical and Electronics Engineers, Inc.
3 Park Avenue
New York, NY 10016-5997
United States of America
stds.info@ieee.org
www.ieee.org

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INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

ICS 25.040.01; 35.060

ISBN 978-2-8322-9974-6

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IEEE Std	FDIS	Report on voting
1800.2 (2017)	91/1713/FDIS	91/1725/RVD

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IEEE Standard for Universal Verification Methodology Language Reference Manual

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Approved 14 February 2017

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Accellera Systems Initiative—*The Universal Verification Methodology (UVM) pre-IEEE Class Reference*.

Abstract: The Universal Verification Methodology (UVM) that can improve interoperability, reduce the cost of using intellectual property (IP) for new projects or electronic design automation (EDA) tools, and make it easier to reuse verification components is provided. Overall, using this standard will lower verification costs and improve design quality throughout the industry. The primary audiences for this standard are the implementors of the UVM base class library, the implementors of tools supporting the UVM base class library, and the users of the UVM base class library.

Keywords: agent, blocking, callback, class, component, consumer, driver, event, export, factory, function, generator, IEEE 1800.2™, member, method, monitor, non-blocking, phase, port, register, resource, sequence, sequencer, transaction level modeling, verification methodology

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Introduction

This introduction is not part of IEEE Std 1800.2-2017, IEEE Standard for Universal Verification Methodology Language Reference Manual.

Verification has evolved into a complex project that often spans internal and external teams, but the discontinuity associated with multiple, incompatible methodologies among those teams can limit productivity. The Universal Verification Methodology (UVM) Language Reference Manual (LRM) addresses verification complexity and interoperability within companies and throughout the electronics industry for both novice and advanced teams while also providing consistency. While UVM is revolutionary, being the first verification methodology to be standardized, it is also evolutionary, as it is built on the Open Verification Methodology (OVM), which combined the Advanced Verification Methodology (AVM) with the Universal Reuse Methodology (URM) and concepts from the ***e*** Reuse Methodology (eRM). Furthermore, UVM also infuses concepts and code from the Verification Methodology Manual (VMM), plus the collective experience and knowledge of the over 300 members of the Accellera UVM Working Group to help standardize verification methodology. Finally, the transaction level modeling (TLM) facilities in UVM are based on what was developed by Open SystemC Initiative (OSCI) for SystemC, though they are not an exact replication or re-implementation of the SystemC TLM library.