

INTERNATIONAL STANDARD

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**Test methods for electrical materials, circuit boards and other interconnection structures and assemblies –
Part 2-720: Detection of defects in interconnection structures by measurement of capacitance**

Méthodes d'essai pour les matériaux électriques, les cartes imprimées et autres structures d'interconnexion et ensembles –

Partie 2-720 : Détection de défauts présents dans les structures d'interconnexion par mesurage de la capacité





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INTERNATIONAL ELECTROTECHNICAL COMMISSION

**TEST METHODS FOR ELECTRICAL MATERIALS, CIRCUIT BOARDS AND
OTHER INTERCONNECTION STRUCTURES AND ASSEMBLIES –****Part 2-720: Detection of defects in interconnection
structures by measurement of capacitance**

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The text of this International Standard is based on the following documents:

Draft	Report on voting
91/1923/FDIS	91/1934/RVD

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

A list of all parts in the IEC 61189 series, published under the general title *Test methods for electrical materials, circuit boards and other interconnection structures and assemblies*, can be found on the IEC website.

Future standards in this series will carry the new general title as cited above. Titles of existing standards in this series will be updated at the time of the next edition.

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TEST METHODS FOR ELECTRICAL MATERIALS, CIRCUIT BOARD AND OTHER INTERCONNECTION STRUCTURES AND ASSEMBLIES –

Part 2-720: Detection of defects in interconnection structures by measurement of capacitance

1 Scope

This part of IEC 61189 provides a method to evaluate specific characteristics of circuit boards by measuring the capacitance between conductor traces and a ground plane and can be used for qualitative comparison of a test specimen to a reference board. This method is not intended for quantitative measurements and for assessment of conformity to a specification.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60194-2, *Printed boards design, manufacture and assembly – Vocabulary – Part 2: Common usage in electronic technologies as well as printed board and electronic assembly technologies*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60194-2 apply. No terms and definitions are listed in this document.

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4 Objective

For testing electrical characteristics of circuit board, generally an electrical open/short test that shall measure the resistance between nets is the main test method. This open/short test is possible only to look at the pass/the fail of circuits and not to look for any reliability issues of circuit board like as mouse bite, delamination, void, and crack. Therefore, the general electrical test has a limitation. Along with the capacitance test method, the electrical test method shall check the existing reliability issues of circuit boards and this standardization of the additional electrical test is necessary from the development stage. It is possible to accurately measure the differences in the capacitance values of circuit boards before and after the reliability test. This is sufficient for the development stage and reliability testing rather than in-production testing because of the long test time of electrical test. Other than the probing contact issues, there is no problem with the measurement uncertainty. It is possible to look for defects such as open/short, mouse bite, delamination, void, and so on by analysing the test defect nets. In looking for the capacitance test method, it shows the capacitance difference depending on the pad width, pad length, and pad distance as shown in Figure 1. Figure 1 shows the defect of mouse bite.

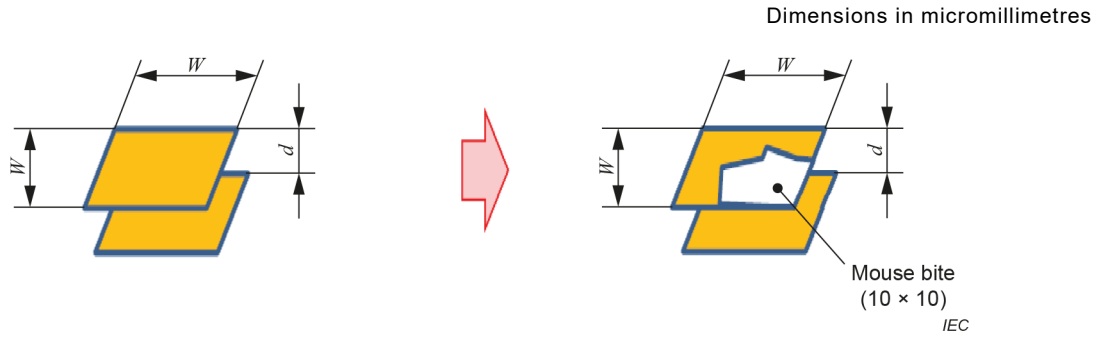


Figure 1 – Capacitance difference depending on the defect of mouse bite

5 Test specimen

Figure 2 shows the test specimen with top test pads and bottom test pads. It shall be prepared to test real circuit boards and test coupons with a warpage specification of less than 2 mm for improving adhesion with the ground metal plate.

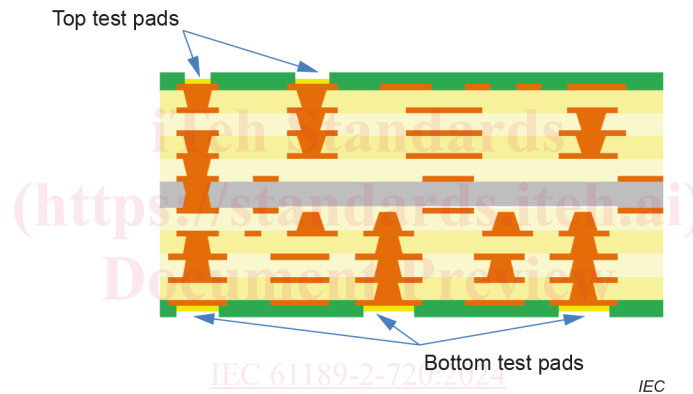


Figure 2 – Test specimen

6 Test method

Figure 3 shows the schematic of the capacitance test method for measuring capacitance using a capacitance tester such as an LCR meter and Impedance tester. After contacting the ground metal plate of one side, the capacitance of all of pads of the other side shall be tested. The top probing tests and the bottom probing tests are conducted.

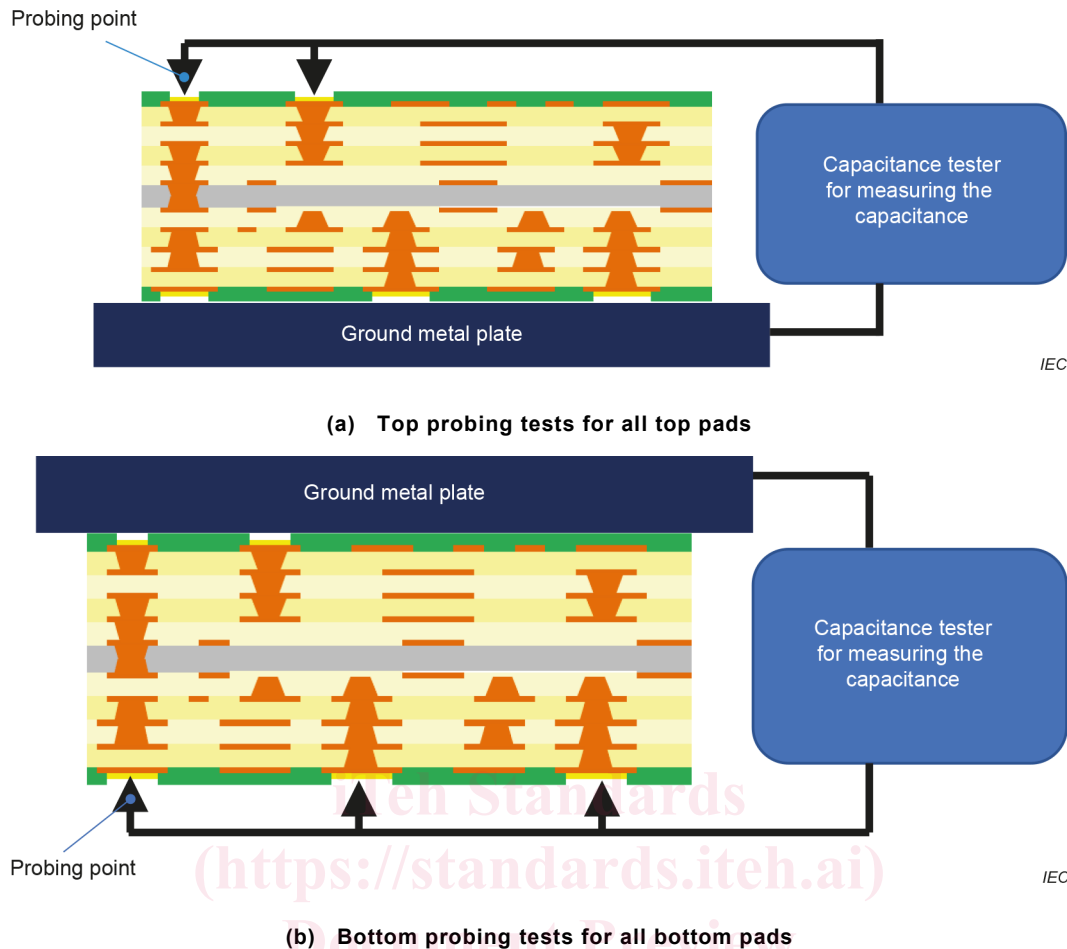


Figure 3 – Schematic of the capacitance test method

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The specimen shall be attached to the ground metal plate without any attached materials, and it may need the ground metal plate with the vacuum suction holes for improving the attachment between test specimen and ground metal plate. The 2-port capacitance tester shall be connected at each probing point and ground metal plate. If looking at the test schematic in Figure A.1, after attaching the test specimen to the ground metal plate, the 2-port impedance tester shall be connected to the pads of the test specimen and ground metal plate. The ground metal plate shall be the common ground and the capacitance shall be measured at each one-side probing point. Also, it is necessary to measure at each other-side probing point. After that, it shall analyze all the test results by comparing the average error ratio of all test specimens.

The test sequences to test the capacitance of circuit boards are as follows:

- 1) Reference board and test specimen shall be kept without packaging at standard laboratory conditions for a minimum of 24 h before measurement.
- 2) Looking for the reference values with the average value for each test pad by testing 10 specimens, then determining the high limit ratio and the low limit ratio.
- 3) Cleaning the contamination on the ground metal plate.
- 4) Putting the test specimen on the ground metal plate and attaching the vacuum suction without any attached materials.
- 5) Firstly, testing the capacitance characteristics of the one-side test specimen with the impedance tester.
- 6) Repeat sequence 2).

- 7) Secondly, attaching the other-side test specimen on the ground metal plate without any attached materials.
- 8) Testing the capacitance characteristics of test specimen with the impedance tester.
- 9) Comparing the capacitance characteristics of all of test results with the average error ratio according to high limit and low limit (referred to in Annex A).

Table 1 – Definition of uppercase

A	B	C	D	E	F
REF-VALUE (F)	MEAS-VALUE (F)	Average error ratio (%)	High LIMIT (%)	Low LIMIT (%)	Judgement (Pass/Failure)

A = the average capacitance value of 10 times testing values

B = the measured capacitance value

$C (\%) = (B/A) * 100$

F(Pass) range = $E \leq C \leq D$

F(Failure) range = $E > C$ or $C > D$

- 10) Judging the pass/failure rate for the electrical characteristics of the circuit board.

8 Report

The test report shall include:

- a) test schematic for the capacitance test method;
- b) measuring frequency;
- c) the impedance tester for measuring the capacitance used;
- d) the ground metal plate as the common ground used;
- e) humidity to room temperature;
- f) the date of the test;
- g) the room temperature under which the test was conducted;
- h) the test sequences;
- i) high limit and low limit;
- j) the table of the average error ratio for comparing all test results;
- k) the pass/failure rate of the circuit board.