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Information technology – High-Performance Parallel Interface –

Part 6: Physical Switch Control (HIPPI-SC)

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CONTENTS

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FOREWORD

1) ISO (International Organization for Standardization) and IEC (International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards through technical committees established by the respective organization to deal with particular fields of technical activity. ISO and IEC technical committees collaborate in fields of mutual interest. Other international organizations, governmental and non-governmental, in liaison with ISO and IEC, also take part in the work.

2) In the field of information technology, ISO and IEC have established a joint technical committee, ISO/IEC JTC1. Draft International Standards adopted by the joint technical committee are circulated to national bodies for voting. Publication as an International Standard requires approval by at least 75 % of the national bodies casting a vote.

3) Attention is drawn to the possibility that some of the elements of this International Standard may be the subject of patent rights. ISO and IEC shall not be held responsible for identifying any or all such patent rights.

International Standard ISO/IEC 11518-6 was prepared by subcommittee 25: Interconnection of information technology equipment, of ISO/IEC joint technical committee 1: Information technology.

This second edition cancels and replaces the first edition published in 1996. The changes are upward compatible and consist mainly of a local address self-discovery method detailed in annex B.3.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 3.

ISO/IEC 11518 consists of the following parts, under the general title *Information technology – High-Performance Parallel Interface:*

– *Part 1: Mechanical, electrical, and signalling protocol specification (HIPPI-PH)*
– *Part 2: Framing Protocol (HIPPI-FP)*
– *Part 3: Encapsulation of ISO/IEC 8802-2 (IEEE Std 802.2) Logical Link Control Protocol Data Units (HIPPI-LE)*
– *Part 4: Mapping of HIPPI to IPI device generic command sets (HIPPI-IPI)*
– *Part 5: Memory Interface (HIPPI-MI)*
– *Part 6: Physical Switch Control (HIPPI-SC)*
– *Part 8: Mapping to Asynchronous Transfer Mode (HIPPI-ATM)*
– *Part 9: Serial Specification (HIPPI-Serial)*

Annexes A and B are for information only.

INTRODUCTION

This part of ISO/IEC 11518 defines the control for HIPPI physical layer switches. HIPPI by itself is an efficient simplex high-performance point-to-point interface. The physical switch control allows the interconnection of multiple HIPPI based equipments with HIPPI physical layer switches.

Characteristics of this HIPPI physical switch control protocol include:

– support for both source routing and destination addresses;

– I-Fields and CCIs can span multiple physical layer switches within a fabric;

– when a Destination end-point receives a packet, it can easily manipulate the I-Field received to return a reply packet to the Source;

– support for physical layer switches with differing numbers of ports, all within the same fabric;

– specified reserved addresses to aid address self-discovery, switch management, and switch control.

INFORMATION TECHNOLOGY – HIGH-PERFORMANCE PARALLEL INTERFACE –

Part 6: Physical Switch Control (HIPPI-SC)

1 Scope

This part of ISO/IEC 11518 specifies a control for physical layer switches using the High-Performance Parallel Interface (HIPPI), a high-performance point-to-point interface between data-processing equipment. This part of ISO/IEC 11518 does not protect against errors introduced by intermediate devices interconnecting multiple HIPPI-PHs.

The purpose of this part of ISO/IEC 11518 is to facilitate the development and use of the HIPPI in computer systems by providing common physical switch control. It provides switch control structures for physical layer switches interconnecting computers, high-performance display systems, and high-performance, intelligent block-transfer peripherals. This part of ISO/IEC 11518 also applies to point-to-point HIPPI topologies.

2 Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this part of ISO/IEC 11518. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this part of ISO/IEC 11518 are encouraged to investigate the possibility of applying the most recent edition of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies. Members of IEC and ISO maintain registers of currently valid International Standards.

ISO/IEC 11518-1:1995, *Information technology – High-Performance Parallel Interface – Part 1: Mechanical, electrical, and signalling protocol specification (HIPPI-PH)*

3 Definitions and conventions

3.1 Definitions

For the purposes of this part of ISO/IEC 11518, the following definitions apply.

3.1.1
connection
condition of the HIPPI-PH when data transfers from a Source end-point to a Destination end-point are possible

3.1.2
connection control information (CCI)
a parameter sent as part of the sequence of operations establishing a connection from a Source to a Destination

3.1.3
end-point
the equipment at either end of the fabric for a particular connection

3.1.4
destination
the equipment at the end of the interface that receives the data

3.1.5
destination end-point
the equipment at the end of the fabric that receives the data

3.1.6
fabric
a group of one or more physical layer switches that can be traversed with one I-Field

3.1.7
I-Field
a 32-bit field that is sent as part of the sequence of the physical layer operations establishing a connection from a Source to a Destination

3.1.8
interface
the set of protocols and control signals used to connect a Source and Destination, as defined by HIPPI-PH

Within a fabric, an interface connects an end-point to a switch or a switch to a neighbouring switch.

3.1.9
Logical Address
an address stored in an I-Field that uniquely identifies a Destination end-point or set of end-points

3.1.10
nibble
a 4-bit entity

3.1.11
optional
features that are not required by this part of ISO/IEC 11518. However, if any optional feature defined by this part of ISO/IEC 11518 is implemented, it shall be implemented according to this part of ISO/IEC 11518

3.1.12
packet
a data set, as defined by HIPPI-PH, sent from Source to Destination. A packet is composed of one or more bursts

3.1.13
physical layer switch
a device which allows a single HIPPI physical layer interface to switch between multiple HIPPI physical layer interfaces without involving protocols above the HIPPI Mechanical, Electrical, and Signalling Protocol Specification (HIPPI physical layer)

3.1.14
source
the equipment at the end of the interface that transmits the data

3.1.15
source Address
an address stored in an I-Field that uniquely identifies a Source end-point or set of end-points

3.1.16
source end-point
the equipment at the end of the fabric that transmits the data

3.1.17
source routing
a means of packet routing whereby the Source end-point specifies the action of each switch on the way to the Destination

3.2 Editorial conventions

In this part of ISO/IEC 11518, certain terms that are proper names of signals, state mnemonics, or similar terms are printed in uppercase to avoid possible confusion with other uses of the same words (for example, REQUEST). Any lowercase uses of these words have the normal technical English meaning.

A number of conditions, sequences, parameters, events, states, or similar terms are printed with the first letter of each word in uppercase and the rest lowercase (for example, Source). Any lowercase uses of these words have the normal technical English meaning.

4 CCI and I-Field formats

4.1 Format

The connection control information (CCI) shall be used for controlling HIPPI physical layer switches. Within ISO/IEC 11518-1 (HIPPI-PH) the CCI is used as the I-Field, and is asserted on the HIPPI-PH Data Bus during a connection sequence. The format of the CCI (I-Field) is shown in figure 1. Examples of CCI and I-Field usage for routing are contained in annex A.

L = Locally Administered (bit 31) = 0 designates that the I-Field is defined by this part of ISO/IEC 11518. L = 1 designates that the rest of the I-Field, bits 30 - 0, are locally administered and are not defined by this part of ISO/IEC 11518.

VU = Vendor_Unique (bits 30,29). The contents of the Vendor_Unique bits are not defined in this part of ISO/IEC 11518. Switches shall pass these bits unmodified to the Destination.

NOTE 1 These bits are available for providing signals to Destinations. Such signals can be used to modify the Destination's behaviour or supply it with additional information on the purpose of the attempted connection.

W = Double-wide (bit 28) = 0 designates that the Source is using the 800 Mbit/s data rate option (DATA BUS is 32 bits wide as defined in HIPPI-PH); the switch shall connect through Cable-A. W = 1 designates that the Source is using the 1 600 Mbit/s data rate option (DATA BUS is 64 bits wide); the switch shall connect through both Cable-A and Cable-B.

NOTE 2 The W bit is used in conjunction with the INTERCONNECT signals on Cable-A and Cable-B. The INTERCONNECT signals, as defined in HIPPI-PH, tell a switch or end-point that the cable is physically attached to an active HIPPI port. The W bit is used to tell the switch, or Destination end-point, whether or not Cable-B is being used in particular connection.

D = Direction (bit 27) = 0, designates that the right-hand end (least significant bits) of the Routing Control field shall be the current sub-field. D = 1 designates that the left-hand end (most significant bits) of the Routing Control field shall be the current sub-field.

NOTE 3 When a reverse path exists, a Destination end-point may return a reply to a received packet by simply using the same I-Field that it received with the D bit complemented. For this to work correctly with source routing (PS = 00) the return path must be symmetrical with the forward path.

PS = Path Selection (bits 26, 25). Used to select either (1) a source route (i.e., a specific route through the switches, with output port numbers specified for each switch) or (2) to specify the Logical Address.

00 = source routing: Source selects the route through the switches.

01 = Logical address: Switches select the first route from a list of possible routes.

10 = reserved

11 = logical address: Switches select a route.

C = Camp-on (bit 24) = 0 specifies that the switch shall reply with a connection reject sequence if unable to complete the connection. C = 1 specifies that the switch shall attempt to establish a connection until either the connection is completed or the Source aborts the connection request.

Camp-on is used by the Source to tell a switch to wait for the selected path (or paths) to become available, i.e., the switch should not generate a rejected connection sequence because the selected path is busy. The algorithm used by a switch to select among multiple Sources camped-on to a single Destination is implementation-specific and is not specified in this part of ISO/IEC 11518.

NOTE 4 A HIPPI rejected connection has a different set of meanings depending on whether or not the Camp-on feature is being used. See clause B.1 for details.

4.2 Source routing

When PS = 00 (i.e., source routing) the Routing Control field shall be split into multiple sub-fields, with the size of each sub-field dependent upon the size of the switch that is using it. The number of bits in the sub-field is described as $[Log_2N]$ where N is the switch size. For example, a 16 by 16 switch would use a 4-bit sub-field.

When D = 0, a switch shall use the current sub-field (right most bits of the Routing Control field) to select the switch output port. The switch shall right shift the Routing Control field by the number of bits in the sub-field, and shall insert the switch input port number in the left most bits of the Routing Control field. See figure 2.

When D = 1, the same actions occur except that the current sub-field shall be at the left end of the Routing Control field. The Routing Control field shall be shifted left, and the input port number shall be inserted at the right end of the Routing Control field. See figure 3.

A switch shall not alter the I-Field except when PS=00, and then, only the Routing Control field shall be modified.

4.3 Logical address

When PS = 01 or 11 (i.e., logical address) the Routing Control field shall be split into two 12-bit fields. One 12-bit field specifies the address of the Destination end-point(s), the other specifies the address of the Source end-point. When the direction D bit = 0, the right-hand 12 bits shall specify the Destination end-points Logical Address and the left-hand 12 bits shall specify the Source end-points Logical Address (see figure 4). When D = 1, the opposite is true (see figure 5).

4.4 Reserved Logical Addresses

Part of the range of logical addresses is reserved to designate the addresses of network services whose location in the network may vary, and for other network management functions. All others are available for assignment to specific Destinations. The logical addresses assigned at the time this part of ISO/IEC 11518 was approved include the following (shown in hexadecimal notation).

NOTE 5 Later registrations will be added as an addendum to this part of ISO/IEC 11518.

F90 – FBF Trial self-discovery addresses. These addresses are reserved for an iterative address self-discovery algorithm. F9x tests the low-order 4-bit nibble, FAx tests the middle 4-bit nibble, and FBx tests the high-order 4-bit nibble, of the switch port's logical address. If the low-order 4-bit nibble of the trial self-discovery address (i.e., the "x" in Fnx) matches the selected nibble in the switch port's logical address, then the switch shall establish a connection back to a HIPPI Destination that is paired with the HIPPI port requesting the connection, i.e., a loopback. If the trial self-discovery nibble values are not equal, the switch shall reject the connection. For example, if the logical address for port "J" is "xyz" where "x", "y", and "z" are 4-bit nibbles, then loopback connections shall be made when trial logical addresses F9"z", FA"y", and FB"x" are used. (See B.3.3 and B.3.5.) Support of this feature is optional.

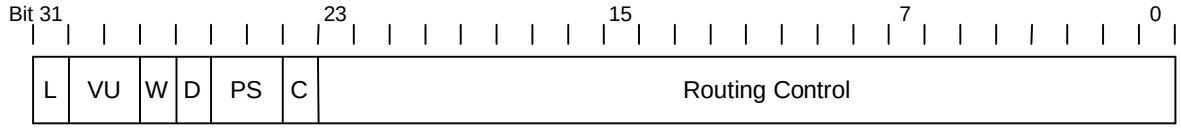

Figure 1 – CCI and I-Field format

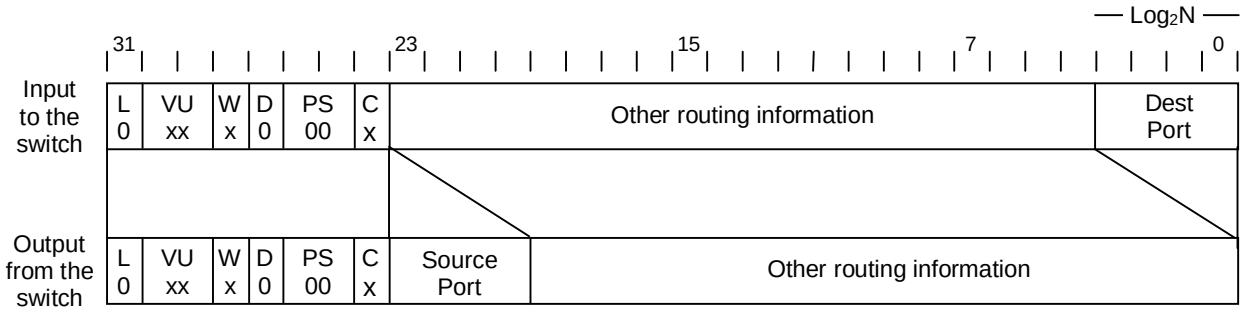

Figure 2 – I-Field with source routing, D = 0, and 16 by 16 switch

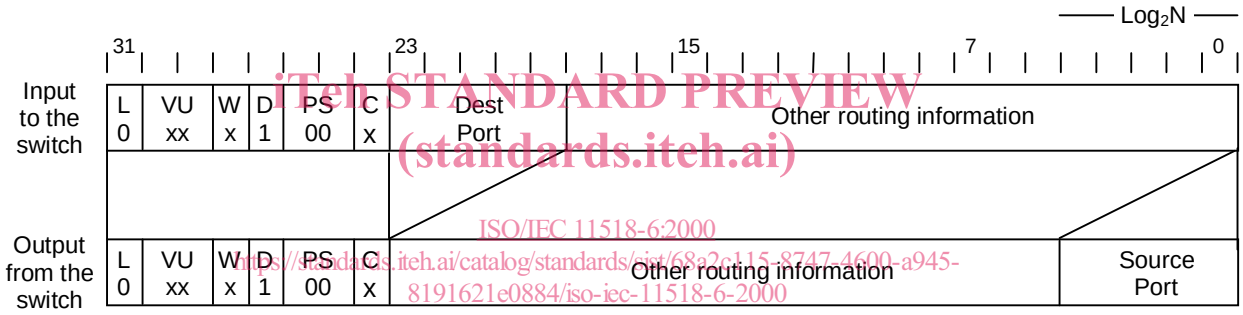

Figure 3 – I-Field with source routing, D = 1, and 32 by 32 switch

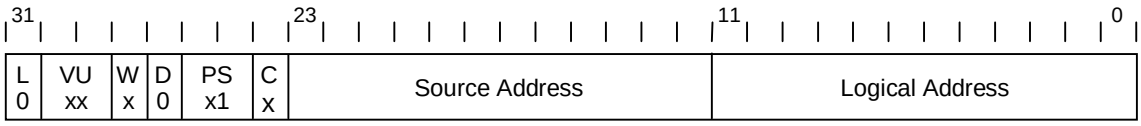

Figure 4 – I-Field with logical addressing and D = 0

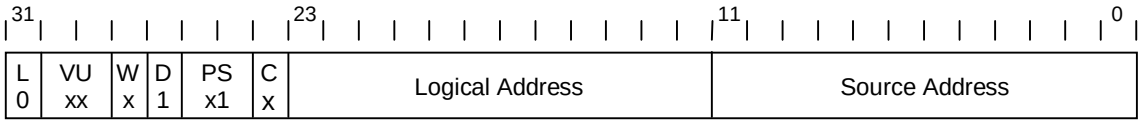

Figure 5 – I-Field with logical addressing and D = 1

FC0 – FDF Reserved for local use

FE0 Messages pertaining to switch configuration, including HIPPI-LE Address Resolution requests as described in RFC 1374 "IP and ARP on HIPPI" [1].

FE1 All IP protocol traffic conventionally directed to the IEEE 802.1 broadcast address as described in RFC 1042 "Standard for IP transmission over 802 networks" [2].

FE2 RFC 1112 Host extensions for IP multicasting Class D addresses not assigned below [3].

FE3 RFC 1131 OSPF specification All Routers (Class D address 224.0.0.5) [4].

FE4 RFC 1131 OSPF specification All Designated Routers (Class D address 224.0.0.6) [4].

FE5 – FE7 Reserved

FE8 ISO/IEC 9542:1988 CLNP ES-IS all ES's [5].

FE9 ISO/IEC 9542:1988 CLNP ES-IS all IS's [5].

FEA ISO/IEC 10589:1992 IS-IS all Level 1 IS's [6].

FEB ISO/IEC 10589:1992 IS-IS all Level 2 IS's [6].

FEC ISO/IEC 15802-3:1998, clause 8, MAC Bridging flooding. [7].

FED ISO/IEC 15802-3:1998, clause 8, Bridging Spanning Tree Protocol. [7].

FEE Embedded switch management agent. Support of this feature is optional.

FEF – FFC Reserved

FFD Loopback logical address for switches to use when probing other switches. Support of this feature is optional.

FFE Loopback logical address for hosts to use when probing switches for the host's logical address. This value is reserved for the establishment of a connection back to a HIPPI Destination that is paired with the HIPPI Source requesting the connection. (See B.3.2 and B.3.5.) Support of this feature is optional.

FFF Unknown or unassigned address. This value should never be used to address a Destination or Destinations. It can be used to indicate that the Source is unaware of its Source Address in the CCI, or to signify an unknown Logical Address in higher layer protocols. A HIPPI-SC switch may alter the I-Field, substituting a valid Source Address for this value. Support for this address substitution is optional. Such substitution may be used to aid in discovery of a system's logical switch address by higher layer protocols. (See B.3.1, B.3.2, and B.3.5.)

The protocols used to access these services and the means whereby these services keep track of their configuration of the network are outside the scope of this part of ISO/IEC 11518.

5 Switch behavior

A HIPPI physical switch has input ports (attachments to HIPPI Sources) and output ports (attachments to HIPPI Destinations). These HIPPI ports shall conform to either the HIPPI-PH or HIPPI-Serial specifications. This clause defines how an HIPPI physical switch behaves with regards to the states of the HIPPI-PH control signals on the input and output ports for a particular connection operation.

5.1 Use of INTERCONNECT signals

As defined in HIPPI-PH, each switch input port and output port shall generate an INTERCONNECT signal when that port is "on-line"; i.e., powered on and enabled for HIPPI connections. Each switch input and output port shall monitor the received INTERCONNECT signal and shall use this signal to validate all other HIPPI control signals.

NOTE 6 A switch port may deassert the INTERCONNECT signal when that port is disabled for maintenance or diagnostics.

5.2 CLOCK signal

The HIPPI CLOCK signal generated by the switch output port (a HIPPI Source) shall be continuous and shall conform to the HIPPI-PH specification at all times.

5.3 Connection request successful

Once a connection is completed the switch shall be transparent, with the exception of switch induced latency, to the HIPPI signal sequences.

NOTE 7 The switch acts as a repeater under the constraints imposed by 7.9 of ISO/IEC 11518-1, and can change the number of idle words between bursts or packets.