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INTERNATIONAL STANDARD

NORME INTERNATIONALE

AMENDMENT 2
AMENDEMENT 2

Power losses in voltage sourced converter (VSC) valves for high-voltage direct current (HVDC) systems – Part 2: Modular multilevel converters

Pertes de puissance dans les valves à convertisseur de source de tension (VSC) des systèmes en courant continu à haute tension (CCHT) – Partie 2: Convertisseurs multiniveaux modulaires

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POWER LOSSES IN VOLTAGE SOURCED CONVERTER (VSC) VALVES FOR HIGH-VOLTAGE DIRECT CURRENT (HVDC) SYSTEMS –

Part 2: Modular multilevel converters

AMENDMENT 2

FOREWORD

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Amendment 2 to IEC 62751-2:2014 has been prepared by subcommittee 22F: Power electronics for electrical transmission and distribution systems, of IEC technical committee 22: Power electronic systems and equipment.

The text of this Amendment is based on the following documents:

Draft	Report on voting
22F/712/CDV	22F/726/RVC

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this Amendment is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications/.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

- reconfirmed,
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3.1.11
no-load operating state

Add, to the end of the existing Note 1 to entry, added by IEC 62751-2/AMD1:2019, the following sentence:

The integration time over which such losses are averaged might need to be longer than during normal operation, so as to obtain the correct weighted average of the losses while blocked and the losses while switching.

4.2 Principles for loss determination

Replace, in the last sentence of the existing first paragraph, modified by IEC 62751-2/AMD1:2019, the word "justify" *with* "explain".

Replace, in the last sentence of the existing third paragraph, modified by IEC 62751-2/AMD1:2019, the text "is now under study in CIGRÉ WG B4-75" *with* "has been studied by CIGRE WG B4-75 and is summarised in Annex C".

Delete the third sentence of the existing last paragraph, starting with "Care should also be taken".

4.4 Loss calculation method

Delete, in the third sentence of the existing first paragraph, the words "for example valve currents and switching energies".

Replace, in the last sentence of the existing second paragraph, the word "currents" *with* "losses".

Delete, in the existing last paragraph, the words "and justified".

Add, to the end of the existing last paragraph, the following new sentence:

The main benefit of the numerical offline simulation is the determination of the average distribution of the switching events across a cycle.

Add, after the existing last paragraph, the following new paragraph:

The remaining calculations can be performed analytically with a reasonable accuracy. If it can be shown by the manufacturer that the distribution of switching events is reasonably accurate, then the remaining calculations shall be allowed to be performed analytically.

4.5.2 Input data for numerical simulations

Replace, in the existing dashed list, modified by IEC 62751-2/AMD1:2019, the first dashed item with the following new item:

The simulation model shall include a control block which reproduces the correct valve current and switching pattern used in the complete system.

*Delete, in the fourth dash of the existing dashed list, modified by IEC 62751-2/AMD1:2019, the words "*parasitic elements*".*

*Replace, in the fifth dash of the existing dashed list, modified by IEC 62751-2/AMD1:2019, the text "*with a reduced number of*" with "*using a lumped representation of the*".*

Delete the last two dashed items of the existing dashed list, modified by IEC 62751-2/AMD1:2019.

Add, after the existing dashed list, modified by IEC 62751-2/AMD1:2019, the following new paragraph and list:

There are two different approaches/methods which may be applied:

1) Two-stage simulation and calculation method on the basis of simulated input values

   In this approach, the input parameters required for a calculation shall be simulated using a model which at least represents the on-state characteristics of the converter as well as the switching pattern or control pattern for the switching of the cells. The on-state representation may be chosen on the basis of worst-case characteristics (at high junction temperatures) or on-state characteristics for lower junction temperatures. The simulated values (voltages, currents and switching pattern) shall be used as input for the calculations. For the calculations with the simulated values, the following two approaches may be used.

   a) The semiconductor parameters are chosen for the rated or worst-case junction temperature condition and the losses shall be calculated on the basis of the rated junction temperature.

      NOTE Due to the assumption of a worst-case temperature condition, this calculation will result in higher losses than what can actually be observed in the real application.

   b) Using a thermal model, the temperature-dependent semiconductor properties shall be considered to calculate the losses for all semiconductors in the converter. Since only steady-state scenarios are the basis for the loss calculation, the thermal heat capacitances may be considered as negligible for the thermal model. The temperature-dependent loss calculation may be executed in an iterative manner. For the iterative calculation approach with the simulation values input, a steady-state condition shall be reached to end the iteration process (as a suggestion ±1 K iteration error border).

2) Loss calculation with an exclusive simulation approach

In this approach, the junction temperature dependent semiconductor properties, such as on-state voltages, and switching and recovery losses, shall be included in the simulation model (i.e. a thermal model shall be included in the simulations, as for the mixed calculation and simulation approach the thermal heat capacitances may be neglected for steady state conditions). The simulation model shall represent the switching pattern or control pattern for the switching of the cells. On the basis of the simulations, the losses shall be extracted directly from the simulation model for all semiconductors in the converter. Similarly to option 1), it is possible to simplify the model by using semiconductor parameters applicable only to the maximum rated junction temperature, but this will result in a more conservative calculation.

4.5.3 Input data coming from numerical simulations

Add, at the end of the existing second paragraph, modified by IEC 62751-2/AMD1:2019, the following sentence:

The required parameters to be derived from the simulations may vary depending on the chosen calculation approach.

4.5.4 Converter station data

Add, in the second dash of the existing paragraph, modified by IEC 62751-2/AMD1:2019, the words ", if any" *after* "filter configuration".

Add, in the third dash of the existing paragraph, modified by IEC 62751-2/AMD1:2019, the words ", if any" *after* "phase reactor inductance".

4.6 Contents and structure of valve loss determination report

Replace, in the existing first paragraph of 4.6, added by IEC 62751-2/AMD1:2019, the words "have been determined and including" *with the words* "have been determined at the project execution stage, including*".*

5.1 General

Add, before the last paragraph, added by IEC 62751-2/AMD1:2019, the following new note:

NOTE When the rated DC current of the HVDC scheme is significantly lower than the rated current of the IGBT, additional measurement points might be necessary in order to obtain acceptable accuracy.

5.2 IGBT conduction losses

Add, at the beginning of the existing first paragraph, the text "Where the piecewise-linear approximation is used,".

Add, at the end of the existing last paragraph, modified by IEC 62751-2/AMD1:2019, the following new sentence:

An analytical approach to calculate the current distribution for the individual submodule elements may be acceptable (e.g. use of switching vector derived from simulation).

Add, after the existing last paragraph, modified by IEC 62751-2/AMD1:2019, the following new paragraph:

For parallel connected semiconductors, the current sharing may be calculated on the basis of the forward characteristics of the semiconductors (usually an equal current sharing).

5.3 Diode conduction losses

Add, at the beginning of the existing first paragraph, the text "Where the piecewise-linear approximation is used,".

Add, at the end of the existing last paragraph, modified by IEC 62751-2/AMD1:2019, the following new sentence:

An analytical approach to calculate the current distribution for the individual submodule elements may be acceptable (e.g. use of switching vector derived from simulation).

Add, after the existing last paragraph, modified by IEC 62751-2/AMD1:2019, the following new paragraph:

For parallel connected semiconductors the current sharing may be calculated on the basis of the forward characteristics of the semiconductors (usually an equal current sharing).

5.4 Other conduction losses

Add, before the last sentence of the existing first paragraph, modified by IEC 62751-2/AMD1:2019, the following new sentence:

The resistances of the busbars shall include not only the internal busbars within the MMC building blocks but also the busbars connecting between MMC building blocks and between the different stacks that make up the valve.

7 Losses in d.c. capacitors of the valve

Delete Note 2.

8.1 General

*Replace, in the last sentence of the existing first paragraph, the words "*control principles*" with "*switching regime*".*

8.2 IGBT switching losses

Add, after the existing last paragraph, the following new paragraph:

For parallel connected semiconductors, the current sharing may be calculated on the basis of the forward characteristics of the semiconductors (usually an equal current sharing).

8.3 Diode switching losses

Add, after the existing last paragraph, the following new paragraph:

For parallel connected semiconductors, the current sharing may be calculated on the basis of the forward characteristics of the semiconductors (usually an equal current sharing).

Annex B Recommended data to be supplied with the loss calculation report

Replace, in the first sentence of the existing first paragraph of Annex B, added by IEC 62751-2/AMD1:2019, the words "facilitate comparisons between reports from different bidders" *with* "explicitly provide the assumptions taken for the loss calculation study".

Replace, in the last sentence of the existing first paragraph of Annex B, added by IEC 62751-2/AMD1:2019, the words "at which losses are subject to financial evaluation" *with* "agreed between manufacturer and purchaser".

Table B.1 – Valve loss data

Add, after the sixth row (reading "13) rms current of IBGT T2 (I_{T2rms})" *under column* "Parameters"*) of Table B.1 of the existing Annex B, added by IEC 62751-2/AMD1:2019, the following new row:*

105) average switching frequency	106)	107)	108)

Replace, in footnote [a] *of Table B.1 of the existing Annex B, added by IEC 62751-2/AMD1:2019, the word* "bidder" *with* "manufacturer".

Add, after the existing Annex B, added by IEC 62751-2/AMD1:2019, the following new annex:

Annex C
(informative)

Loss measurement

As transmission losses are directly related to the investment and operational costs, they are one of the most important factors for high voltage direct current (HVDC) project evaluation. For voltage source converters (VSC), valve losses are the largest part of the total converter station losses and therefore the determination and evaluation of the VSC valve losses becomes highly important.

At the time of writing of this Annex C, the losses of VSC valves are determined based on the calculation methods of IEC 62751-1 and IEC 62751-2. The calculation method requires detailed information, such as the parameters of semiconductor devices, VSC valve design characteristics and operating modes, which are usually not directly available to the HVDC system purchaser or user, who consequently finds it difficult to evaluate the calculated losses results.

Therefore, CIGRÉ working group B4-75 was set up in 2017 to perform a feasibility study to assess laboratory loss measurement methods on VSC valves for loss calculation evaluation purposes and to make recommendations considering the pros and cons of such measurement methods versus the methods in IEC 62751. The results of this working group were published in 2021 as CIGRÉ TB 844.

The brochure starts with a general description of losses in VSC HVDC converter valves, the origins of different losses in components, the dependency of the losses on different operating modes, as well as special aspects of different designs. This is followed by a summary of the current practice for valve losses determination, including the modelling of the semiconductor parameters and then by a discussion on how the transparency of the overall calculation process can be enhanced. As the main study results of the WG B4-75, an evaluation of the existing methods to measure losses is provided. This is complemented by an overview of the operation conditions and additional aspects for losses measurement (such as commercial aspects) that need to be taken into account. In the last part, the results are summarized and recommendations for application of losses measurement are given, which can be used as guidance for the introduction of losses measurements in the operational type tests of VSC valves.

The conclusion of TB 844 is that the laboratory measurement of valve losses is feasible, although the level of accuracy achievable is still quite poor. The general recommendation therefore is that the laboratory measurement should become a standard part of the operational type tests of the VSC valves, such that in the coming years greater industry experience can be gained in this area. However, it is not recommended that the measured valve losses are used as part of the financial evaluation criteria for the HVDC project, until there is a good level of industry experience and consensus over what should be a realistically achievable level of measurement uncertainty.

Bibliography

Replace the existing reference "CIGRÉ WG B4-75, *Feasibility study for assessment of lab losses measurement of VSC valves*" *with the following new reference:*

CIGRÉ Technical Brochure 844, *Feasibility study for assessment of lab losses measurement of VSC valves*, WG B4-75

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