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INTERNATIONAL STANDARD

NORME INTERNATIONALE

Single crystal wafers for surface acoustic wave (SAW) device applications – Specifications and measuring methods

Tranches monocristallines pour applications utilisant des dispositifs à ondes acoustiques de surface (OAS) – Spécifications et méthodes de mesure

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SINGLE CRYSTAL WAFERS FOR SURFACE ACOUSTIC WAVE (SAW) DEVICE APPLICATIONS – SPECIFICATIONS AND MEASURING METHODS

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IEC 62276 has been prepared by IEC technical committee 49: Piezoelectric, dielectric and electrostatic devices and associated materials for frequency control, selection and detection. It is an International Standard.

This fourth edition cancels and replaces the third edition published in 2016. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

a) The terms and definitions, the technical requirements, sampling frequency, test methods and measurement of transmittance, lightness, colour difference for LN and LT have been added in order to meet the needs of industry development;

b) The term “inclusion” (mentioned in 4.13 and 6.10) and its definition have been added because there was no definition for it in Clause 3;

c) The specification of LTV and PLTV, and the corresponding description of sampling frequency for LN and LT have been added, because they are the key performance parameters for the wafers;

d) The tolerance of Curie temperature specification for LN and LT have been added in order to meet the development requirements of the industry;

e) Measurement of thickness, TV5, TTV, LTV and PLTV have been completed, including measurement principle and method of thickness, TV5, TTV, LTV and PLTV.

The text of this International Standard is based on the following documents:

Draft	Report on voting
49/1454/CDV	49/1460/RVC

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

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- withdrawn, or
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SINGLE CRYSTAL WAFERS FOR SURFACE ACOUSTIC WAVE (SAW) DEVICE APPLICATIONS – SPECIFICATIONS AND MEASURING METHODS

1 Scope

This document applies to the manufacture of synthetic quartz, lithium niobate (LN), lithium tantalate (LT), lithium tetraborate (LBO), and lanthanum gallium silicate (LGS) single crystal wafers intended for use as substrates in the manufacture of surface acoustic wave (SAW) filters and resonators.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60758:2016, *Synthetic quartz crystal – Specifications and guidelines for use*

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

- IEC Electropedia: available at https://www.electropedia.org/
- ISO Online browsing platform: available at https://www.iso.org/obp

3.1 Flatness

3.1.1

fixed quality area

FQA

central area of a wafer surface, defined by a nominal edge exclusion, X, over which the specified values of a parameter apply

Note 1 to entry: The boundary of the FQA is at all points (e.g. along wafer flats) the distance X away from the perimeter of the wafer of nominal dimensions as shown in Figure 1.

3.1.2

reference plane

plane used as a reference for flatness measurements

Note 1 to entry: The reference plane can be one of the following types:

a) for measurements in which the wafer is clamped, the reference plane is the flat chuck surface that is identical with the back surface of the wafer;

b) for measurements in which the wafer is not clamped, the reference plane is defined by the surface height at three points on the front surface of the wafer within the FQA;

c) for measurements in which the wafer is not clamped, the reference plane is defined by the least-squares fit to the front surface of the wafer using the surface height at all measured points within the FQA.

3.1.3
site

square area on the front surface of the wafer with one side parallel to the OF

Note 1 to entry: Flatness parameters are assessed either globally for the FQA, or for each site individually.

3.1.4
TV5

thickness variation for five points

difference between the maximum thickness and the minimum thickness at the centre and four peripheral points of the wafer as shown in Figure 1

Dimensions in millimetres

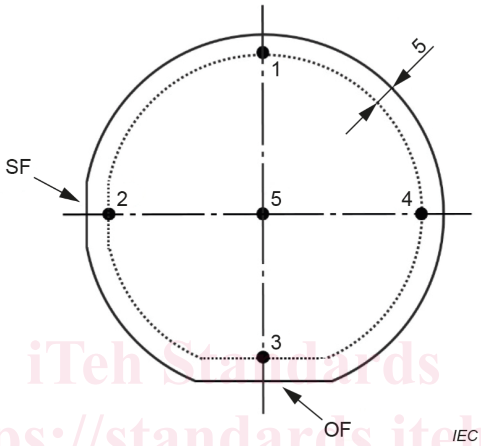


Figure 1 – Wafer sketch and measurement points

3.1.5
TTV

total thickness variation

difference between the maximum thickness d_1 and the minimum thickness d_2 of a wafer as shown in Figure 2

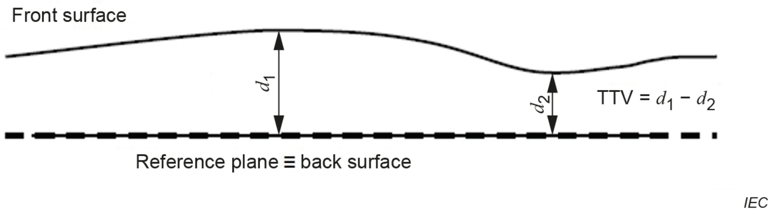


Figure 2 – Schematic diagram of a TTV

Note 1 to entry: Measurement of TTV is performed on a clamped wafer with the reference plane as defined in 3.1.2 a).

3.1.6
warp

maximum distance between the highest point and the lowest point on the front surface of an unclamped wafer from the reference plane, where the three-point reference plane is used

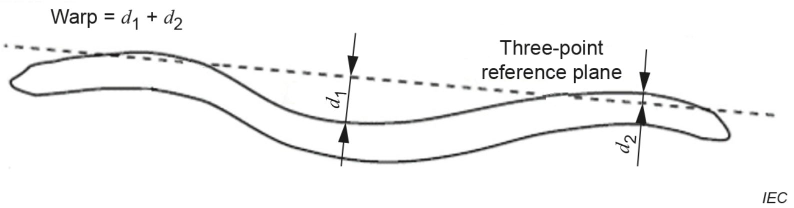


Figure 3 – Schematic diagram of a warp

Note 1 to entry: The warp describes the deformation of a wafer that is not clamped, as shown in Figure 3.

Note 2 to entry: The reference plane is defined by the surface height at three points on the front surface of the wafer as described in 3.1.2 b).

3.1.7
sori

maximum distance between the highest point and the lowest point on the front surface of an unclamped wafer from the reference plane, where the least-squares fit reference plane is used

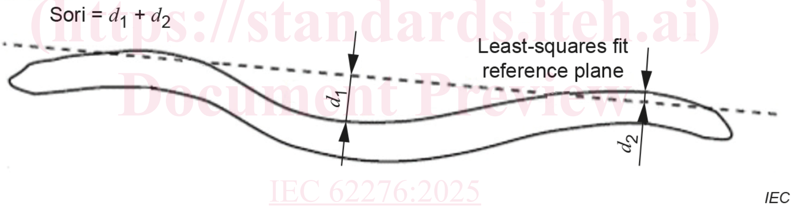


Figure 4 – Schematic diagram of a sori

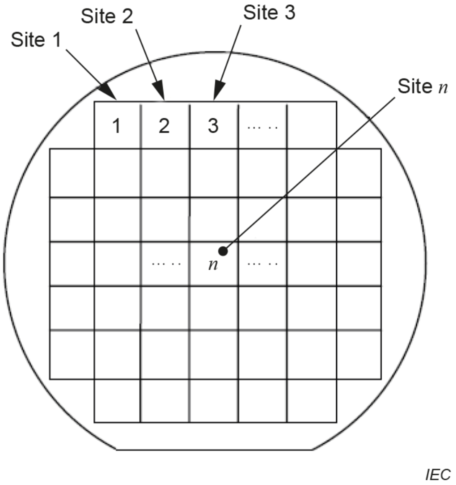
Note 1 to entry: The sori describes the deformation of a wafer that is not clamped, as shown in Figure 4.

Note 2 to entry: The reference plane is defined by the least-squares fit to the front surface of the wafer as described in 3.1.2 c).

3.1.8
LTV

local thickness variation

difference between the maximum value and the minimum value of a wafer thickness at each site of the wafer surface



Note 1 to entry: All sites existing within the fixed quality area (FQA) on the wafer surface possess their own LTV value.

Figure 5 – Example of the distribution of sites for measurement of the LTV

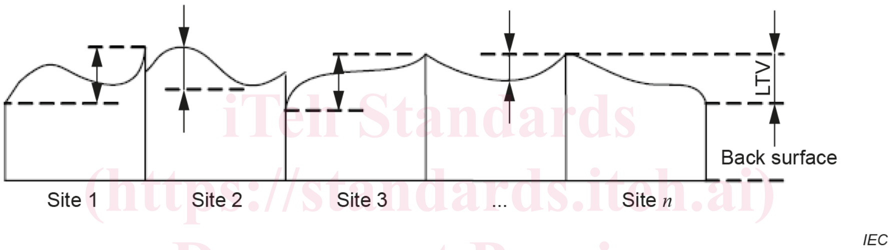


Figure 6 – LTV defined within each site on the wafer surface

Note 2 to entry: Measurement is performed on a clamped wafer with the reference plane as defined in 3.1.2 a). An example of the distribution of sites for measurement of the LTV is shown in Figure 5. The LTV is defined within each site, as illustrated in Figure 6.

3.1.9
PLTV

percent local thickness variation

percentage of sites whose local thickness variation values fall within the specified value

Note 1 to entry: As with the LTV, measurement is performed on a clamped wafer with the reference plane defined in 3.1.2 a).

3.1.10
FPD

focal plane deviation

maximum distance between a point on the wafer surface within the fixed quality area and the three-point reference plane

Note 1 to entry: The three-point reference plane is defined in 3.1.2 b).

Note 2 to entry: If the point on the wafer surface is above the three-point reference plane, the FPD is positive. If that point is below the three-point reference plane, the FPD is negative.

3.2 Appearance defects

3.2.1
contamination
foreign matter on a surface of wafer which cannot be removed after cleaning

3.2.2
crack
fracture that extends to the surface of the wafer and that can or cannot penetrate the entire thickness

3.2.3
scratch
shallow groove or cut below the established plane of the surface, with a length to width ratio greater than 5:1

3.2.4
chip
region where material has been removed from the surface or edge of the wafer

Note 1 to entry: The size of a chip can be expressed by its maximum radial depth and peripheral chord length.

3.2.5
dimple
smooth surface depression larger than 3 mm diameter

3.2.6
pit
non-removable surface anomaly

EXAMPLE A hollow, typically resulting from a bulk defect or faulty manufacturing process.

3.2.7
orange peel
pear skin
large-featured, roughened surface visible to the unaided eye under diffuse illumination

3.3 Other terms and definitions

3.3.1
manufacturing lot
lot established by agreement between the customer and the supplier

3.3.2
orientation flat
OF
flat portion of a wafer perimeter indicating the crystal orientation

Note 1 to entry: Generally, the OF corresponds to the SAW propagation direction (see Figure 1).

3.3.3
secondary flat
SF
flat portion of a wafer perimeter shorter than the orientation flat

Note 1 to entry: When present, the SF indicates wafer polarity and can serve to distinguish different wafer cuts (see Figure 1).

3.3.4
back surface roughness
roughness that scatters and suppresses spurious bulk waves at the back surface of a wafer

3.3.5
surface orientation
crystallographic orientation of the axis perpendicular to the polished surface of the wafer

3.3.6
description of orientation and SAW propagation
indication of the surface orientation and the SAW propagation direction, separated by the symbol "-"

Note 1 to entry: Specification of a 0° orientation is normally omitted.

Note 2 to entry: Description of wafer orientation rule is shown in Annex A.

3.3.7
tolerance of surface orientation
maximum permissible angular deviation of the surface orientation measured by X-ray diffraction from the specified surface orientation

3.3.8
bevel
slope of the perimeter edge of a wafer

Note 1 to entry: The process of forming a slope is called "bevelling".

Note 2 to entry: Machining of the perimeter edge of a wafer can be performed through bevelling or edge rounding. Whereas bevelling produces a flat slope, edge rounding (as the term implies) produces a rounded edge.

Note 3 to entry: Both bevelling and edge rounding, and their tolerances, are subject to agreement between the user and the supplier.

3.3.9
diameter of wafer
diameter of circular portion of wafer excluding the OF and SF regions

3.3.10
wafer thickness
thickness measured at the centre of the wafer

3.3.11
inclusion
foreign material (solid, liquid or vapor) within a piezoelectric crystal, detectable by examination of scattered light

3.3.12
electrical twins in synthetic quartz wafer
synthetic quartz wafer in which regions with the common Z-axis exist showing a polarity reversal of the electrical X-axis

Note 1 to entry: Electrical twins can result from extreme conditions (temperature and pressure, for example) during processing.

3.4 Terms and definitions related to LN and LT wafers

3.4.1
colour difference
ΔE_{ab}^{*}
difference in colour at different parts of the object surface