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INTERNATIONAL STANDARD

NORME INTERNATIONALE

Semiconductor devices – Mechanical and climatic test methods – Part 5: Steady-state temperature humidity bias life test

Dispositifs à semiconducteurs – Méthodes d'essais mécaniques et climatiques – Partie 5: Essai continu de durée de vie sous température et humidité avec polarisation

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INTERNATIONAL
ELECTROTECHNICAL
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SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 5: Steady-state temperature humidity bias life test

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IEC 60749-5 has been prepared by IEC technical committee 47: Semiconductor devices. It is an International Standard.

This third edition, based on JEDEC document JESD22-A101D.01, cancels and replaces the second edition published in 2017. It is used with permission of the copyright holder, JEDEC Solid State Technology Association. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

a) the specification of the test equipment is changed to require the need to minimize relative humidity gradients and maximize air flow between semiconductor devices under test;

b) the specification of the test equipment fixtures is changed to require the avoidance of condensation on devices under test and on electrical fixtures connecting the devices to the test equipment;

c) replacement of references to “virtual junction” with “die”.

The text of this International Standard is based on the following documents:

Draft	Report on voting
47/2820/FDIS	47/2827/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

A list of all parts of the IEC 60749 series, under the general title *Semiconductor devices – Mechanical and climatic test methods*, can be found in the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn, or
- revised.

SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 5: Steady-state temperature humidity bias life test

1 Scope

This part of IEC 60749 provides a steady-state temperature and humidity bias life test to evaluate the reliability of non-hermetic packaged semiconductor devices in humid environments.

This test method is considered destructive.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60749-4, *Semiconductor devices – Mechanical and climatic test methods – Part 4: Damp heat, steady-state, highly accelerated stress test (HAST)*

3 Terms and definitions

No terms and definitions are listed in this document.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

- IEC Electropedia: available at https://www.electropedia.org/
- ISO Online browsing platform: available at https://www.iso.org/obp

4 General

Temperature, humidity and bias conditions are applied to accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it.

Where both this steady-state, humidity bias test and the damp heat, highly accelerated stress test (HAST) of IEC 60749-4 are performed, the results of this 85 °C/85 % RH steady-state test will take priority over the results of the HAST test, which is an accelerated test designed to activate the same failure mechanisms.

5 Equipment

5.1 Equipment summary

The test requires a temperature-humidity test chamber capable of maintaining a specified temperature and relative humidity continuously, while providing electrical connections to the devices under test in a specified biasing configuration.

5.2 Temperature and relative humidity

The chamber shall be capable of providing controlled conditions of temperature and relative humidity during ramp-up to, and ramp-down from the specified test conditions.

The test chamber dry bulb temperature shall exceed the wet bulb temperature at all times.

5.3 Devices under stress

Devices under stress shall be physically located to minimize temperature gradients. Devices under test shall be physically located in order to minimize relative humidity gradients and maximize air flow between devices.

5.4 Minimizing release of contamination

Board and socket materials shall be chosen in order to minimize release of contamination, and to minimize degradation due to corrosion and other mechanisms.

5.5 Ionic contamination

The test devices shall be placed in the test apparatus to minimise ionic contamination from items such as the card cage, test boards, sockets, wiring and storage containers.

5.6 Deionized water

Deionized water with a minimum resistivity of 1 × 104 Ωm at room temperature shall be used.

6 Test conditions

6.1 Test conditions summary

Test conditions consist of a temperature, relative humidity, and duration used in conjunction with an electrical bias configuration specific to the device.

6.2 Temperature, relative humidity and duration

Unless otherwise required by the detail specification, the temperature, relative humidity and test duration as shown in Table 1 shall be applied.

Table 1 – Temperature, relative humidity and duration

Temperature (dry bulb) °C	**Relative humidity** [a] %	**Temperature** [b] **(wet bulb)** °C	**Vapour pressure** [b] kPa	**Duration** [c] h
85 ± 2	85 ± 5	81,0	49,1	$1\ 000\ {}^{-24}_{+168}$

[a] Tolerances apply to the entire useable test area.

[b] For information only.

[c] The test conditions are to be applied continuously, except during any interim readouts, when the devices should be returned to stress within the time specified in 7.6.

6.3 Biasing guidelines

Apply bias according to the following guidelines:

a) minimize power dissipation;

b) alternate pin bias as much as possible;

c) distribute potential differences across chip metallization as much as possible;

d) maximize voltage within operating range;

NOTE The priority of the above guidelines depends on the mechanism and specific device characteristics.

e) either of two kinds of bias can be used to satisfy these guidelines, whichever is more severe:

1) Continuous bias

The DC bias shall be applied continuously.

Continuous bias is more severe if the die temperature (T_j) is <10 °C higher than the chamber ambient temperature.

If the die temperature is not known, and the heat dissipation of the device under test (DUT) is less than 200 mW, the die temperature is assumed to be less than 10 °C above ambient temperature.

If the heat dissipation of the DUT exceeds 200 mW, the die temperature should be calculated or measured.

If the die temperature exceeds the chamber ambient temperature by more than 5 °C, the rise of the die temperature above the chamber ambient should be included in reports of test results since acceleration of failure mechanisms will be affected.

2) Cycled bias

The DC voltage applied to the devices under test shall be periodically interrupted with an appropriate frequency and duty cycle. If the biasing configuration results in a temperature rise above the chamber ambient, ΔT_{ja}, exceeding 10 °C, then cycled bias, when optimized for a specific device type, will be more severe than continuous bias. Heating as a result of power dissipation tends to drive moisture away from the die and thereby hinders moisture-related failure mechanisms. Cycled bias permits moisture collection on the die during the off periods when device power dissipation does not occur. Cycling the DUT bias with 1 h on and 1 h off is optimal for most plastic-encapsulated microcircuits. The die temperature, as calculated on the basis of the known thermal impedance and dissipation should be quoted with the results whenever it exceeds the chamber ambient by 5 °C or more.

6.4 Biasing choice and reporting

Criteria for choosing continuous or cyclical bias, and whether or not to report the amount by which the die temperature exceeds the chamber ambient temperature, are summarized in Table 2.

Table 2 – Criteria for choosing continuous or cyclical bias

ΔT_{ja}	Continuous or cyclical bias	Include value of ΔT_{ja} in test report?
ΔT_{ja} < 5 °C or power per DUT < 200 mW	Continuous	No
(ΔT_{ja} ≥ 5 °C or power per DUT ≥ 200 mW), and ΔT_{ja} < 10 °C	Continuous	Yes
ΔT_{ja} ≥ 10 °C	Cyclical [a]	Yes

[a] Cycling the DUT bias with one hour on and one hour off is optimal for most plastic-encapsulated microcircuits.

7 Procedures

7.1 Mounting

The test devices shall be mounted in such a way as to expose them to a specified condition of temperature and humidity as given in Table 1 with a specified electrical biasing condition. Exposure of devices to excessively hot conditions, dry ambient conditions or conditions that result in condensation on devices and electrical fixtures shall be avoided, particularly during ramp-up and ramp-down. Appropriate attention should also be made to avoid any water dripping on the devices under stress.

7.2 Ramp-up

The time to reach stable temperature and relative humidity conditions shall be less than 3 h. Condensation on the devices under stress and/or fixtures/hardware shall be avoided at all times by ensuring that their temperature is always higher than the dew point temperature.

7.3 Ramp-down

Ramp-down shall not exceed 3 h. Condensation shall be avoided by ensuring that the test chamber (dry bulb) temperature exceeds the wet-bulb temperature at all times during ramp down.

NOTE For a DUT with a cavity in the package, condensation can occur due to the length of the ramp down time.

7.4 Test clock

The test clock starts when the temperature and relative humidity reach the set points, and stops at the beginning of ramp-down.

7.5 Bias

Bias application during ramp-up and ramp-down is optional. Bias should be verified after devices are loaded, prior to the start of the test clock. Bias should also be verified after the test clock stops, but before devices are removed from the chamber.

7.6 Read-out

An electrical test shall be performed not later than 48 h after the end of ramp-down.

For intermediate read-outs, devices shall be returned to stress within 96 h of the end of ramp-down. Moisture loss can be reduced by placing the device in sealed moisture barrier bags (without desiccant). When devices are placed in sealed bags, the “test window clock” runs at one-third of the rate of devices exposed to laboratory ambient conditions. Thus, the test window can be extended to as much as 144 h, and the time to return to stress to as much as 288 h by enclosing the devices in moisture-proof bags.

The electrical test parameters should be chosen to preserve any defect (i.e. by limiting the applied test current).

Additional time-to-test delay or the return-to-stress delay time is allowed if justified by technical data.

7.7 Handling

Suitable hand-covering shall be used to manage devices, boards and fixtures. Contamination control is important in any accelerated moisture stress test.