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CAMAC - SERIAL HIGHWAY INTERFACE SYSTEM

Système CAMAC - Interface pour Interconnexion de Branche Série

CAMAC-System - Serielle Ringleitung

BODY OF THE HD

The Harmonization Document consists of:

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The English and French versions of this Harmonization Document are provided by the text of the IEC publication and the German version is the official translation of the IEC text. The German translation is not yet available.

According to the CENELEC Internal Regulations the CENELEC member National Committees are bound :

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by or before 1986-07-01

to publish their new harmonized national standard
by or before 1987-07-01

to withdraw all conflicting national standards
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CAMAC – Serial Highway Interface System

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CAMAC — SERIAL HIGHWAY INTERFACE SYSTEM

FOREWORD

1) The formal decisions or agreements of the IEC on technical matters, prepared by Technical Committees on which all the National Committees having a special interest therein are represented, express, as nearly as possible, an international consensus of opinion on the subjects dealt with.

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4) The IEC has not laid down any procedure concerning marking as an indication of approval and has no responsibility when an item of equipment is declared to comply with one of its recommendations.

PREFACE

This standard has been prepared by IEC Technical Committee No. 45, Nuclear Instrumentation.

The Advisory Committee on Electronics and Telecommunications (ACET) has recommended that Technical Committee No. 45 should be responsible for the introduction of IEC standards based on features of the CAMAC standard interface.

This standard defines a serial highway interface system for use with CAMAC crate-assemblies in accordance with IEC Standard 516 and with other controlled devices. It is based on the Standards IEEE 595 and EUR 6100e, as developed by the NIM Committee of the U.S. Energy Research and Development Administration and the ESONE Committee of European Laboratories. A parallel highway interface system, also intended for use with IEC Publication 516, is defined in IEC Publication 552. Other devices and buses, such as that of IEC Publication 625-1, can be readily incorporated into the CAMAC system through an interfacing module.

A first draft was discussed at the meeting held in Milan in 1974. As a result of the meeting held in Baden-Baden in 1977, a draft, Document 45(Central Office)111, was submitted to the National Committees for approval under the Six Months' Rule in November 1977.

The National Committees of the following countries voted explicitly in favour of publication:

Belgium	Japan	Switzerland
Canada	Netherlands	Turkey
Egypt	Poland	Union of Soviet Socialist Republics
Finland	Romania	United Kingdom
France	South Africa (Republic of)	United States of America
Germany	Spain	
Italy	Sweden	

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Note. — Standard IEC symbols will be introduced systematically in all figures in later editions, as feasible.

Other IEC publications quoted in this standard:

Publications Nos. 516: A Modular Instrumentation System for Data Handling; CAMAC System.
552: CAMAC — Organization of Multi-crate Systems. Specification of the Branch-Highway and CAMAC Crate Controller Type A1.
625-1: An Interface System for Programmable Measuring Instruments (Byte serial, Bit parallel), Part 1: Functional Specifications, Electrical Specifications, Mechanical Specifications, System Applications and Requirements for the Designer and User.

CAMAC — SERIAL HIGHWAY INTERFACE SYSTEM

SECTION ONE — GENERAL

1. Scope

This standard is applicable to a certain interface system called CAMAC Serial Highway System, designed to be used as a standard interface between a number of CAMAC measuring instruments, display units, control units, actuators, data processing equipment (computers) and communication equipment.

The Serial Highway System is essentially a unidirectional loop used to circulate byte-organized* messages, and to which are connected a System Controller and up to 62 CAMAC crate-assemblies, in accordance with IEC Publication 516: A Modular Instrumentation System for Data Handling: CAMAC System, or other controlled devices. The highway transfers data and control information in either bit-serial mode (using one data signal and a bit-clock signal) or byte-serial mode (using eight data signals and a byte-clock signal). Clock rates up to 5 MHz may be used, depending on individual system characteristics.

In the primary application, the controlled devices are CAMAC crate assemblies, with Serial Crate Controllers which conform to a defined message structure. In this application the Serial Highway is intended to complement the Parallel Highway defined in IEC Publication 552, CAMAC Organization of Multi-crate Systems. Specification of the Branch Highway and CAMAC Crate Controller Type A1.

This system will be attractive in certain applications that the Parallel Highway was not designed to cover, for example, where there are long distances between crates, or where simplicity of interconnections is desirable. However, the time required to perform a complete operation, including a Dataway cycle, will generally be longer in a serial system than on the Parallel Highway.

The Serial Highway System is defined primarily in terms of the message format and signal standards at the input and output ports of devices connected to the highway. Interconnections between devices may be made directly, using the defined signal standards, or indirectly through communications channels with other signal standards and types of modulation.

This standard also applies partly to controlled devices connected to the Serial Highway, not necessarily constructed in CAMAC format or controlled by CAMAC commands.

Serial Crate Controllers conforming to the full specification and devices conforming to a certain subset of the full specification can co-exist on the highway without mutual interference.

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* In this standard, the French term *caractère* and the English word "byte" are equivalent. The definition is that of ISO 2382/IV, term 04-02-01.

2. Object

To describe and specify the CAMAC Serial Highway System. To define the message formats and signal standards.

This standard is supplementary to the standards laid down in IEC Publication 516 and should be read in conjunction with that publication. No part of this standard is intended to supersede or modify IEC Publication 516.

This standard:

a) lays down mandatory requirements;

b) defines recommended or preferred practices, to be followed unless there are sound reasons to the contrary;

c) gives examples of permitted practices.

The Serial Crate Controllers referred to in this standard are not necessarily interchangeable. Appendix A, however, defines a Serial Crate Controller, Type L2, in a more restrictive way, so that units produced by different manufacturers to this specification are operationally interchangeable.

In order to *conform* with this standard, an equipment or a system shall satisfy all the mandatory requirements included in this publication, except the appendices. If constructed as a CAMAC plug-in unit, the equipment shall also satisfy the mandatory requirements of IEC Publication 516.

In order to *conform* with the standard specification of the CAMAC Serial Crate Controller, Type L2, equipment shall satisfy all the mandatory requirements of Appendix A.

In order to be *compatible* with this standard, equipment need not satisfy all the mandatory requirements, provided it does not interfere with the full operation of all the features of the Serial Highway and of the Serial Crate Controller (including Type L2) as defined in this standard.

This standard is not intended to exclude the use of compatible equipment (in the above sense), even if it does not conform fully to this standard or is not constructed as CAMAC plug-in units.

3. Terminology: Interpretation of this standard

In this standard there are mandatory requirements, recommendations and examples of permitted practice.

Mandatory clauses of the standard are written in bold type as here, and usually include the word *shall*.

Definitions of recommended or preferred practice (to be followed unless there are sound reasons to the contrary) include the word *should*.

Examples of permitted practice generally include the word *may*, and leave freedom of choice to the designer or user.

4. Abbreviations and symbols

The following abbreviations and symbols are used in this standard (list, page 17).

The single letter designations L, M, N, P and R (prefixed in some cases by "CC") are reserved for future use in connection with this standard and shall not be used, except as later assigned.

Abbreviations and Symbols

A	SUB-ADDRESS (Dataway signal)*
ACL	Auxiliary Controller Lockout
B	BUSY (Dataway signal)*
BCK	Byte Clock
C	CLEAR (Dataway signal)*
CBY	CONTROLLER BUSY
DSBY	Demand Busy
DERR	Delayed Error
DMI	Demand Message Initiate
DSQ	DELAYED Q RESPONSE
DSX	DELAYED COMMAND ACCEPTED RESPONSE
ERPT	External Repeat
ERR	Error bit
I	INHIBIT (Dataway signal)*
L	Look-at-Me (Dataway signal)*
LAM	Look-at-Me (Demand)
LSB	Least Significant bit
MI	Message Identification
MSB	Most Significant bit
N	Station Number (Dataway signal)*
NRZL	Non-Return-to-Zero-Level
PH	Parallel Highway of IEC Publication 552
Q	Response, Status (Dataway signal)*
S	Prefix for Serial Highway fields and bits
S1	STROBE (Dataway signal)*
S2	STROBE (Dataway signal)*
SA	Sub-address bit
SC	Crate address bit
SCC	Serial Crate Controller
SCC-L2	Serial Crate Controller, Type L2
SD	Serial Driver
SF	Function bit
SGL	Serial Graded LAM (Demand)
SGLE	DEMAND MESSAGE bits from SGL Encoder
SH	Serial Highway of this standard
SLP	Selected-LAM Present
SN	STATION NUMBER bit
SQ	Q-Response bit
SR	Read bit
STIM	Start Timer
SW	Write bit
SX	COMMAND ACCEPTED bit
T	Clock period
TIMO	Time-out
X	Command accepted (Dataway signal)*
Z	Initialize (Dataway signal)*

* See IEC Publication 516.

SECTION TWO — PRINCIPLES OF THE SERIAL HIGHWAY SYSTEM

This section summarizes the basic principles that apply to all devices connected to the Serial Highway (SH). All other sections of this standard are concerned with the primary applications, where the connected devices are CAMAC crate-assemblies with Serial Crate Controllers.

5. Configuration

The Serial Highway interconnects a master device (the Serial Driver) and up to 62 CAMAC crate-assemblies or other controlled devices. At any time there is only one active master device, but the standard does not exclude systems in which more than one device is capable of acting as master. Figure 1, page 27, shows the basic configuration.

The addressing scheme allows a maximum of 62 controlled devices, whose assigned addresses need not be related to the actual sequence of devices along the highway.

The Serial Highway (SH) forms a unidirectional loop from the output port of the Serial Driver (SD), through each controlled device in turn, and back to the input port of the Serial Driver. (When describing conditions with respect to a particular device, it is often convenient to use the term "upstream" to refer to the part of the SH between the output port of the SD and the device, and the term "downstream" to refer to the part between the device and the input port of the SD.)

6. Messages

All messages transmitted on the Serial Highway consist of sequences of 8-bit bytes as shown in Figure 2, page 27. All information related to the message is contained within these 8-bit bytes.

The eight bits constituting a byte are labelled Bit 1 (least significant) to Bit 8 (most significant). In all bytes, Bits 1 to 6 are available for information fields.

Bit 7 of every byte is a DELIMITER bit, which allows receiving devices to identify the first and last bytes of each message.

Bit 8 is available for use as an odd-parity bit (with appropriate value so that the byte contains an odd number of bits in the logic "1" state). It is always used in this way in the first and last bytes of a message, and in all bytes of messages associated with CAMAC Serial Crate Controllers.

Every message starts with a "HEADER" byte. This includes a device address (a Crate Address when the device is a Serial Crate Controller). In a message from the SD, the Header byte contains the address of the destination. In a message to the SD, it contains the address of the source. Bit 7 of the HEADER byte is at logic "0" and Bit 8 conserves odd parity over the whole byte.

Every message ends with a DELIMITER byte, in which Bit 7 is at logic "1" and Bit 8 conserves odd parity.

The length and content of the "text" between the HEADER byte and the DELIMITER byte of a message can be chosen to suit the needs of the individual device. In principle, it need not be uniform for all devices in a system. In each byte between the HEADER byte and the DELIMITER byte, Bit 7 is at logic "0".

If there are any bytes between the DELIMITER byte of one message and the HEADER byte of the next, they are also DELIMITER bytes with Bit 7 at logic "1".

Thus, the HEADER byte of a message can be identified because, after one or more bytes with Bit 7 at logic "1", it is the first byte with Bit 7 at logic "0". Similarly, the last byte of a message can be identified because, after one or more bytes with Bit 7 at logic "0", it is the first byte with Bit 7 at logic "1".

Error detection over a block of bytes constituting a message or part of a message can be provided by the combination of byte-parity in Bit 8 of each byte and a set of columns-parity bits in bits 1 to 6 of the last byte of the block. This "Geometric Error-Detection Code" detects all 1-bit, 2-bit and 3-bit errors, and most errors with 4 or more bits. The scheme offers good protection against bursts of errors and is easy to implement by hardware or software.

7. Transmission of bytes

Bytes are transmitted either in bit-serial mode (using one data signal and an accompanying bit-clock signal) or in byte-serial mode (using eight data signals and an accompanying byte-clock signal). In bit-serial mode, the 8-bit byte is transmitted with the least significant bit (bit 1) first. It is preceded by a START bit (logic "0") and followed by a STOP bit and optional PAUSE bits (logic "1") as shown in Figure 3, page 29. The START and STOP bits form a byte-frame from which receiving devices can recover a byte-clock.

In the text of this standard, the bit-pattern of an 8-bit byte with least significant bit "*l*" and most significant bit "*m*" is represented by the bit string $(miiiiiil)_2$. The same byte with START and STOP bits is represented by the bit string $(1,miiiiiil,0)_2$.

The message structure and protocol of the Serial Highway are identical in the two modes of transmission.

Throughout a Serial Highway System, bytes are transferred in synchronism with the byte-clock, which accompanies the data in byte-serial mode and is derived from the byte-framing in bit-serial mode.

In each byte-clock period, each device receives one byte and transmits one byte, but the contents (bits 1 to 8) of the received and transmitted bytes are not always identical. Devices normally retransmit the contents of all received bytes, although the contents of a byte received in one byte-period may be retransmitted in a later byte-period. A device can generate a message by interrupting this process of retransmission. The contents of the required number of bytes are generated by the device, and the contents of a corresponding number of received bytes are not retransmitted. The message protocol should ensure that these received bytes do not contain important information. For example, they may be SPACE or WAIT bytes as defined in Section Three.