INTERNATIONAL STANDARD

IEC 61883-1

Second edition
2003-01

Consumer audio/video equipment – Digital interface –

Part 1: General

Matériel audio/vidéo grand public – Interface numérique –

Partie 1: Généralités

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

CONSUMER AUDIO/VIDEO EQUIPMENT – DIGITAL INTERFACE –

Part 1: General

FOREWORD

1) The IEC (International Electrotechnical Commission) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of the IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, the IEC publishes International Standards. Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. The IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
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International Standard IEC 61883-1 has been prepared by technical area 4, Digital system interfaces, of IEC technical committee 100: Audio, video and multimedia systems and equipment.

This second edition of IEC 61883-1 cancels and replaces the first edition, published in 1998, of which it constitutes a technical revision.

The text of this standard is based on the following documents:

FDIS	Report on voting
100/557/FDIS	100/609/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

International Standard IEC 61883 consists of the following parts under the general title *Consumer audio/video equipment – Digital interface:*

Part 1: General

Part 2: SD-DVCR data transmission

Part 3: HD-DVCR data transmission

Part 4: MPEG2-TS data transmission

Part 5: SDL-DVCR data transmission

Part 6: Audio and music data transmission protocol

Part 7: Transmission of ITU-R BO.1294 System B

The committee has decided that the contents of this publication will remain unchanged until 2005. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

CONSUMER AUDIO/VIDEO EQUIPMENT – DIGITAL INTERFACE –

Part 1: General

1 Scope

This part of IEC 61883 specifies a digital interface for consumer electronic audio/video equipment using IEEE 1394, High Performance Serial Bus. It describes the general packet format, data flow management and connection management for audio-visual data, and also the general transmission rules for control commands.

The object of this standard is to define a transmission protocol for audio-visual data and control commands which provides for the interconnection of digital audio and video equipment, using IEEE 1394.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEEE 1212:2001, *Standard for a Control and Status Registers (CSR) Architecture for microcomputer buses*

IEEE 1394:1995, *Standard for a High Performance Serial Bus*

IEEE 1394a:2000, *Standard for a High Performance Serial Bus – Amendment 1*

NOTE Throughout this document, the term "IEEE 1394" indicates a reference to the standard that is the result of the editorial combination of IEEE 1394:1995 and IEEE 1394a:2000. Devices conforming solely to IEEE 1394:1995 may conform to IEC 61883. Devices conforming to IEC 61883 should conform to IEEE 1394a:2000.

3 Abbreviations

For the purpose of this part of IEC 61883, the following abbreviations apply:

AV/C	Audio Video Control
CHF	CIP Header Field
CIP	Common Isochronous Packet
CMP	Connection Management Procedures
CSR	Command and Status Register
CTS	Command/Transaction Set
CRC	Cyclic Redundancy Check Code
DVCR	Digital Video Cassette Recorder
EOH	End of CIP Header
FCP	Function Control Protocol
iPCR	Input Plug Control Register
iMPR	Input Master Plug Register
MPEG	Motion Picture Experts Group
oPCR	Output Plug Control Register
oMPR	Output Master Plug Register
ROM	Read Only Memory

4 High performance serial bus layers

4.1 Cable physical layer

All cable physical layer implementations conforming to this standard shall meet the performance criteria specified by IEEE 1394. Either the cable and connector defined in IEEE 1394:1995, or the cables and connector defined in IEEE 1394a:2000, shall be used.

When necessary for an AV device to generate a bus reset, it shall follow the requirements of IEEE 1394a:2000, 8.2.1. An AV device that initiates a bus reset should generate an arbitrated (short) bus reset, as specified by IEEE 1394a:2000, in preference to the long bus reset defined by IEEE 1394:1995.

4.2 Link layer

All link layer implementations conforming to this standard shall meet the specifications of IEEE 1394.

4.3 Transaction layer

All transaction layer implementations conforming to this standard shall meet the specifications of IEEE 1394.

5 Minimum node capabilities

A node shall conform to the following requirements:

– a node shall be cycle master capable. This is because every node has the possibility to be assigned as a root;

– a node shall be isochronous resource manager capable, as specified by IEEE 1394:1995, and shall implement the additional isochronous resource manager facilities and responsibilities specified by IEEE 1394a:2000 in subclauses 8.3.1.5, 8.3.2.3.8, 8.3.2.3.11, 8.4.2.3 and 8.4.2.6A;

– a node which transmits or receives isochronous packets shall have plug control registers (see 7.2).

5.1 Serial bus management

Bus manager capability is optional for AV devices, but, if implemented by devices conforming to this standard, shall conform to IEEE 1394.

5.2 Command and status registers

5.2.1 CSR core registers

This standard conforms to the CSR architecture. Details of its registers are specified by IEEE 1394.

The STATE_CLEAR.*cmstr* bit shall be implemented as specified by IEEE 1394a:2000, 8.3.2.2.1.

NOTE The *cmstr* bit is set automatically (see IEEE 1394a:2000, 8.3.2.2.1) by system software or hardware when a node becomes the new root after the bus reset process is completed. In this manner, it is possible to ensure the fast resumption and continuity of data transmission where the time scale is critical at the level of microseconds. The rapid activation of a new cycle master decreases the likelihood of a gap in the transmission of cycle start packets; uninterrupted transmission of cycle start packets at nominal 125 µs intervals is critical to the delivery of isochronous data within its latency requirements.

5.2.2 Serial bus node registers

Implementation requirements for bus-dependent registers in this standard conform to IEEE 1394. A node shall have the following registers:

CYCLE_TIME register

BUS_TIME register

BUS_MANAGER_ID register

BANDWIDTH_AVAILABLE register

CHANNELS_AVAILABLE register

A node should have the following register specified by IEEE 1394a:2000:

BROADCAST_CHANNEL register

5.2.3 Configuration ROM requirements

A node shall implement the general ROM format as defined in IEEE 1212:2001 and IEEE 1394. Additional information required for implementations of this standard shall be included in one of the unit directories. Figure 1 shows an example of the configuration ROM implementation for this standard.

5.2.3.1 Bus_Info_Block entry

Implementation requirements for the Bus_Info_Block in this standard shall conform to IEEE 1394.

5.2.3.2 Root directory

The following entries shall be present:

– Module_Vendor_ID;

– Node_Capabilities;

– Unit_Directory (offset to a unit directory defined by this standard).

Other entries may be implemented in addition to the above required entries.

5.2.3.3 Unit directory

The following entries shall be present:

– Unit_Spec_ID;

– Unit_SW_Version.

The value of the Unit_Spec_ID and the Unit_SW_Version for this standard are given as follows:

Unit_Spec_ID:	First octet	= 00_{16}
	Second octet	= $A0_{16}$
	Third octet	= $2D_{16}$
Unit_SW_Version:	First octet	= 01_{16}

The second and third octets of Unit_SW_Version for this standard are specified in Table 9 and indicate capabilities for command/transaction sets. The Unit_SW_Version field is used to identify which protocol is supported by the device. If a device supports more than one protocol, the device shall have a separate unit directory for each protocol supported.

6 Real time data transmission protocol

6.1 Common isochronous packet (CIP) format

6.1.1 Isochronous packet structure

The structure of the isochronous packet utilized by this standard is illustrated in Figure 2. The packet header and header CRC are the first two quadlets of an IEEE 1394 isochronous packet. The CIP header is placed at the beginning of the data field of an IEEE 1394 isochronous packet, immediately followed by zero or more data blocks.

6.1.2 Packet header structure

The packet header consists of the following items as specified in IEEE 1394.

Data_length: specifies the length of the data field of the isochronous packet in bytes, which is determined as follows:

CIP header size + signal data size

Tag: provides a high level label for the format of data carried by the isochronous packet.

00_2 = No CIP header included

01_2 = CIP header included as specified in 6.1.3

10_2 = Reserved

11_2 = Reserved

Channel: specifies the isochronous channel number for the packet.

Tcode: specifies the packet format and the type of transaction that shall be performed (fixed at 1010_2).

Sy: application-specific control field.

6.1.3 CIP header structure

The CIP header is placed at the beginning of the data field of an IEEE 1394 isochronous packet. It contains information on the type of the real time data contained in the data field following it. The structure of the CIP header is shown in Figure 3.

The definitions of the fields are given as follows:

EOH_n (End of CIP header): means the last quadlet of a CIP header.

0 = Another quadlet will follow

1 = The last quadlet of a CIP header

Form_n: in combination with EOH, shows the additional structure of CHF_n.

CHF_n (CIP header field): CIP header field of n^{th} quadlet. The additional structure of CHF_n depends on EOH_0, form_0, EOH_1, form_1, ... EOH_n, and form_n.

6.2 Transmission of fixed length source packet

This protocol transfers a stream of source packets from an application on a device to an application on other device(s). A source packet is assumed to have a fixed length, which is defined for each type of data. The data rate can be variable.

A source packet may be split into 1, 2, 4 or 8 data blocks, and zero or more data blocks are contained in an IEEE 1394 isochronous packet. A receiver of the packet shall collect the data blocks in the isochronous packet and combine them to reconstruct the source packet to send to the application.

A model conforming to these requirements is shown in Figure 4.

6.2.1 Two-quadlet CIP header (form_0=0, form_1=0)

This standard defines the two-quadlet CIP header for a fixed length source packet. There are two types for the structure of the two-quadlet CIP header as shown in Figure 5. One is the CIP header with SYT field (Figure 5a), and the other is the CIP header without SYT field (Figure 5b). If a device transmits real time data (identified by FMT) and requires time stamp in the CIP header, it shall use the SYT format.

The definitions of the fields are given as follows.

– SID: Source node ID (node ID of transmitter).

– DBS: Data block size in quadlets.

DBS field is 8 bits because 256 quadlets is the maximum payload size for S100 mode. When 8 bits are all 0, it means 256 quadlets; and 00000001_2 to 11111111_2 means 1 quadlet to 255 quadlets accordingly.

00000000_2 = 256 quadlets
00000001_2 = 1 quadlet
00000010_2 = 2 quadlets
....
11111111_2 = 255 quadlets

Several data blocks may be put into a bus packet, which is a packet to be transmitted on the bus, if a higher bandwidth is required for S200 and S400 speed.

NOTE S100, S200 and S400 are transmission speeds as defined in IEEE 1394.

– FN: Fraction number.

The number of data blocks into which a source packet is divided. The allowable numbers and allocated FN codes are listed in Table 1.

– QPC: Quadlet padding count (0 quadlet to 7 quadlets).

The number of dummy quadlets padded at the end of every source packet to enable division into equally sized data blocks. The value of all bits in padding quadlets is always zero.

The number of padding quadlets shall be less than the number of data blocks into which every source packet is divided, as encoded by FN.

The number of padding quadlets shall be less than the size of a single data block, as encoded by DBS. Consequently, a data block shall never consist entirely of padding quadlets.

– SPH: Source packet header.

The value one indicates that the source packet has a source packet header. The format of the source packet header is shown in Figure 6. Code allocation of the time stamp field is shown in Table 4. When a time stamp is indicated, the time stamp field shall be encoded as the lower 25 bits of the IEEE 1394 CYCLE_TIME register. Other bits are reserved for future extension and shall be zeros.