SLOVENSKI STANDARD

SIST HD 431 S1:2003

april 2003

Block transfers in CAMAC system

ICS 27.120.99; 35.240.99

Referenčna številka
SIST HD 431 S1:2003(en)

CENELEC
GENERAL SECRETARIAT
Rue Bréderode 2, Bte 5 - 1000 BRUXELLES
Tel. 02 - 511 79 32 - Telex 26257 Cenlec b

HD 431

ENGLISH VERSION

UDC: 621.039-791.1 621.317.39::621.039 621.38.084::514.13
681.3.01-887
Key words: Nuclear instrumentation - electrical measurements of nuclear technology quantities - modular construction of electronic instruments - transfer of data groups

BLOCK TRANSFERS IN CAMAC SYSTEMS

Transferts de bloc dans les systèmes CAMAC

Block-Übertragungen in CAMAC-Systeme

BODY OF HD

The Harmonization Document consists of:

- **IEC 677 (1980 - 1st edition - IEC TC 45),** not appended

This Harmonization Document was approved by CENELEC on **7 July 1982.**

The English and French versions of this HD are provided by the text of the IEC publication and the German version is the official translation of the IEC text which is not yet available.

According to the CENELEC Internal Regulations the CENELEC member National Committees are bound:

to announce the existence of this Harmonization Document at national level

by or before **1982-07-07**

to publish their new harmonized national standard

by or before **1983-06-01**

to withdraw all conflicting national standards

by or before **1984-01-01.**

Harmonized national standards are listed on the HD information sheet, which is available from the CENELEC National Committees or from the CENELEC General Secretariat.

The CENELEC National Committees are the national electrotechnical committees of Austria, Belgium, Denmark, Finland, France, Germany, Greece, Ireland, Italy, Luxemburg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, United Kingdom.

NORME INTERNATIONALE

INTERNATIONAL STANDARD

CEI
IEC
60677

Première édition
First edition
1980-01

Transferts de bloc dans les systèmes CAMAC

Block transfers in CAMAC systems

International Electrotechnical Commission 3, rue de Varembé Geneva, Switzerland
Telefax: +41 22 919 0300 e-mail: inmail@iec.ch IEC web site http: //www.iec.ch

Commission Electrotechnique Internationale
International Electrotechnical Commission
Международная Электротехническая Комиссия

CODE PRIX
PRICE CODE R

Pour prix, voir catalogue en vigueur
For price, see current catalogue

CONTENTS

Page

FOREWORD 5

PREFACE 5

Clause

1. Scope and object 7
   1.1 Scope 7
   1.2 Object 7

2. Introduction and classification 7
   2.1 Introduction 7
   2.2 Classification of Block Transfer Modes 9

3. Block Transfer Modes described in IEC Publication 516 15
   3.1 UCS (Stop) Mode 15
   3.2 ACA (Address Scan) Mode 15
   3.3 UQC (Repeat) Mode 17

4. Additional Block Transfer Modes 17
   4.1 UCW (Stop-on-Word) Mode 19
   4.2 ULS (LAM Synchronized Stop) Mode 19
   4.3 UDS (Direct Synchronized Stop) Mode 21
   4.4 MCA (Multi-device Action) Mode 21

5. Compatibility 23
   5.1 Block Transfer Mode MCA 25
   5.2 Block Transfer Modes XCX, XLX, XDX 25
   5.3 Block Transfer Modes ULS, UDS, ULC, UDC, UQC 25
   5.4 Block Transfer Modes ULS, UDS, ULW, UDW 25

6. Hardware design 27
   6.1 Module design — Q Response 27
   6.2 Module design — LAM Signal 31
   6.3 Interface design 33

7. Software considerations 35

APPENDIX A — Other Block Transfer Mode 37

Tables:

I. Block Transfer Mode descriptor 11
II. Block Transfer Names 11
III. Compatibility Aspects of Stop and Stop-on-Word Block Transfer Termination Modes 23
IV. Single module, Single Address Block Transfer: Recommended Method for Performing UCS (Stop) Mode and corresponding LAM Synchronized CAMAC Block Transfers 27
V. Recommended Method for Performing ACA (Address Scan) and UQC (Repeat) Mode CAMAC Block Transfers . 29
VI. Method for Performing UCW (Stop-on-Word) Mode and Corresponding LAM Synchronized CAMAC Block Transfers 31

FIG. 1. — Recommended implementation of a Module's LAM Signal which is intended for Block Transfer Synchronization. Simplified Block Diagram 33

INTERNATIONAL ELECTROTECHNICAL COMMISSION

BLOCK TRANSFERS IN CAMAC SYSTEMS

FOREWORD

1) The formal decisions or agreements of the IEC on technical matters, prepared by Technical Committees on which all the National Committees having a special interest therein are represented, express, as nearly as possible, an international consensus of opinion on the subjects dealt with.

2) They have the form of recommendations for international use and they are accepted by the National Committees in that sense.

3) In order to promote international unification, the IEC expresses the wish that all National Committees should adopt the text of the IEC recommendation for their national rules in so far as national conditions will permit. Any divergence between the IEC recommendation and the corresponding national rule should, as far as possible, be clearly indicated in the latter.

PREFACE

This standard has been prepared by IEC Technical Committee No. 45: Nuclear Instrumentation.

A first draft was discussed at the meeting held in Nice in 1978. As a result of this meeting, a draft, Document 45(Central Office)129, was submitted to the National Committees for approval under the Six Months' Rule in May 1979.

The National Committees of the following countries voted explicitly in favour of publication:

Australia
Austria
Belgium
Canada
Czechoslovakia
Egypt
Finland
France
Germany
Italy
Netherlands
Poland
South Africa (Republic of)
Spain
Sweden
Turkey
Union of Soviet Socialist Republics
United States of America

Other IEC publications quoted in this standard:

Publications Nos. 516: A Modular Instrumentation System for Data Handling; CAMAC System.
552: CAMAC—Organization of Multi-crate Systems. Specification of the Branch-highway and CAMAC Crate Controller Type A1.

Other publication: IML: A Language for use in CAMAC Systems, ESONE/IML/01, October 1974, ESONE Secretariat, and TID-26615, January 1975, DOE, Washington, D.C., U.S.A.

BLOCK TRANSFERS IN CAMAC SYSTEMS

1. Scope and object

1.1 *Scope*

This standard covers requirements for subroutines for CAMAC systems as defined in IEC Publication 516: A Modular Instrumentation System for Data Handling; CAMAC System. Its application shall not conflict or cause conflict with the mandatory requirements of IEC Publication 516.

1.2 *Object*

Recommendations are presented for uniform practice with regard to block transfers in CAMAC modular instrumentation and digital interface systems of IEC Publication 516.

2. Introduction and classification

2.1 *Introduction*

The basic CAMAC specification, IEC Publication 516, defines a single CAMAC operation as the activity which occurs in response to a single CAMAC command. This activity may consist of the transfer of a single data word between a CAMAC module and computer memory or the changing of the status of a module (for example F(26), F(24)) or return of a value for Q as the result of a test made on the module, or any compatible set of the previously named activities. A block transfer is defined as a sequence of single CAMAC operations involving data which the user specifies by a command said to be of a higher level than one which specifies a single CAMAC operation. The higher-level command contains all the information required for the specification of the desired sequence of single CAMAC commands and is interpreted by a channel which governs the activity on the CAMAC highway. Control information, such as the readiness of the computer to participate in a data transfer, the state of the CAMAC Q line and the state of certain LAMs or special synchronizing signals must be made available to the channel. The use made of the control information by the channel defines the block transfer mode. If a module is to influence the sequence of operations within a block transfer, then it must have the features required by the particular mode.

A channel consists of an interface to the CAMAC system as well as a means for selecting and executing the algorithms of the block transfer modes that are implemented. An algorithm may be implemented wholly in hardware or wholly in software or by a combination of hardware and software. The possibility of software implementation of any algorithm means that CAMAC block transfers can take place on a system which does not have the hardware (such as direct memory access) required to carry out "computer" block transfers. Note that a module behaves in the same way when it is accessed by a hardware algorithm as it does when accessed by conventional programmed computer input-output. Regardless of the method of channel implementation, the use of the channel results in reductions in both the CPU time required and the programming effort, through the use of predefined algorithms.

Many different block transfer algorithms (or modes) may be defined, all of which are compatible with the CAMAC specifications. It is also possible to have a channel execute a sequence of CAMAC commands which does not involve the transfer of data. An example of such a "Multiple Action" mode is discussed in Appendix A. Many algorithms use control information conveyed by either a Q or an L signal or both. The requirements placed on these signals by one algorithm may conflict with those placed on them by another algorithm. Hence compatibility problems between modes and channels can occur. This is especially true if no restrictions are placed on the choice of a suitable block transfer algorithm. However, experience with many different CAMAC systems and extensive analysis of the problem has revealed that a restricted number of block transfer algorithms can satisfy nearly all needs. To encourage uniformity in future designs of modules and controllers, certain algorithms are recommended to be used whenever possible and some additional algorithms are suggested for special applications that cannot practicably be implemented with the recommended algorithms. The possibility remains for a user to define other block transfer algorithms to meet special needs.

In the following clauses, the recommended block transfer algorithms are discussed. In Clause 3, those given in IEC Publication 516 are described. These algorithms are well established and are supported by existing hardware, both in modules and in CAMAC interfaces available for many small computers. Clause 4 discusses the new algorithms.

The CAMAC user is reminded that the block transfer characteristics of the modules, the controller (branch driver or computer-crate interface), and the software in the computer must be matched in order for the block transfer algorithms to be carried out correctly. The ability to perform block transfers is a feature of the total computer system and its interfaces.

2.2 *Classification of Block Transfer Modes*

The various block transfer modes can be classified by specifying the nature of each of three fundamental characteristics—how the CAMAC address is determined, the source of the synchronizing signal, and the method used to terminate the block transfer. In the following clauses, these characteristics are described and a notation permitting a compact specification of the various modes is defined.

The notation is based on the use of a single letter to represent the nature of each characteristic. The letters are written in the order that the characteristics were mentioned above and the resulting three letters completely describe a block transfer mode. If a certain characteristic need not be specified, then it is denoted by the letter X. Thus the symbol XXX describes a block transfer mode in which all the characteristics are undefined. Table I summarizes the meaning of each letter used and Table II lists the modes described in this document, the corresponding terms in IEC Publication 516 and the IML language definition.

2.2.1 *CAMAC Address Sequencing*

The first letter of the block transfer mode descriptor indicates the method used to determine the CAMAC address of the next CAMAC operation.

A block transfer accessing a CAMAC address which stays constant during the block transfer is typically used to access a buffer within a module or to access an external device (such as a computer peripheral unit) through a CAMAC module. Such Uni-Address block transfers are denoted by the letter U.

TABLE I

Block Transfer Mode descriptor

First letter —	*CAMAC address sequencing:*	
	U	Uni-Address
	M	Multi-Address — see calculated and given address arrays in IML
	A	Address Scan
	E	Extended Address Scan
Second letter —	*Synchronizing source:*	
	C	Controller
	Q	Q Response
	L	Look-at-Me (LAM) Signal
	D	Pseudo-LAM Signal
Third letter —	*Operation termination:*	
	C	Channel Word Count
	A	Terminal Address Reached
	S	Q = 0 on last + one word
	W	Q = 0 on last word
	L	Look-at-Me (LAM) Signal
	D	Pseudo-LAM Signal

TABLE II

Block Transfer Names

Descriptor	IEC Publication 516	IML
UCS	Stop Mode	UBC
UCW	None	UBC
UQC	Repeat Mode	UBR
ACA	Address Scan Mode	MAD
MCA	None	MA
ULS	None	UBL
UDS	None	UBL
ULW	None	UBL
UDW	None	UBL

A block transfer accessing a sequence of CAMAC addresses is typically used to access a set of registers located at different places within a CAMAC system but containing related data. The algorithm for determining the next CAMAC address may depend on the state of Q resulting from the last operation.

The Address Scan (ACA) Mode described in Sub-clause 5.4.3.1 of IEC Publication 516 is the main example of this technique, although there is a variant, the Extended Address Scan (ECA) Mode, which is described in Appendix A.

The sequence of CAMAC addresses may also be determined either by a list of all the addresses or by the parameters: starting address, increments to be applied to each part of the address, and final address. These correspond to the Given and Calculated Arrays of CAMAC addresses in IML and both are indicated by the letter M for Multi-Address.

2.2.2 *Synchronization source*

The second letter of a block transfer mode descriptor indicates the source of synchronization of individual transfers. In some cases the module is continuously ready to effect a transfer and the channel controller may execute the CAMAC commands at any convenient rate. The block transfer is then said to be "controller synchronized", and the descriptor for all such modes is of the form XCX.

In other cases the module is not continuously ready. Following a particular transfer a certain time must elapse before it can effect another. The rate at which the block transfer proceeds is controlled by the module (or modules). Hence the module must provide synchronization information to the channel so that it can correctly execute its part of the block transfer process. For such "module synchronized" block transfers, three sources of synchronizing signal have been identified. They are:

1) the Q response as in the Repeat Mode (see Sub-clause 5.4.3.2 of IEC Publication 516) denoted by Q;

2) a specific Dataway Look-at-Me (LAM) signal, denoted by L;

3) a special signal (Pseudo-LAM) sent directly from the module to the controller, denoted by D.

2.2.3 *Block Transfer Termination*

The third and final letter of a block transfer mode descriptor indicates the means by which the block transfer is terminated. A given block transfer may be halted by either the channel or the module, depending on the conditions existing at the time of the action. It is assumed that all block transfers will be executed with a limit on the number of transfers permitted; in addition to this channel word-count limit there may be other conditions occurring either in the channel or the module which will terminate the transfer. The first such condition to occur terminates the process.

If a block transfer can be terminated only by exhausting a word count within the channel, it is designated by the letter C. If a block transfer can be terminated by the channel either because a word count is exhausted or because a sequence of addresses in a multi-address transfer is exhausted, it is designated by the letter A.

A block transfer can also be terminated by a status signal from the module. While either an L signal or a special signal sent directly to the channel could be used, all the module terminated modes described in this document use the Q response associated with each CAMAC operation of the block transfer.

In Sub-clause 5.4.3.3 of IEC Publication 516 such a mode is described. A response Q = 1 is interpreted as meaning that the operation took place within the block. The first response Q = 0 indicates that the end of block occurred on the previous operation. In IEC Publication 516 this is called the Stop mode and is designated here by the letter S.

Another possible interpretation of a response Q = 0 is that it accompanies the last operation in the block. For write commands, the data word has been accepted by the module and for read command the data word has been transferred to the computer. This is the Stop-on-Word mode and is designated by the letter W.