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IPC-6016

Qualification and Performance Specification for High Density Interconnect (HDI) Layers or Boards

IPC-6016

May 1999

A standard developed by IPC

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

QUALIFICATION AND PERFORMANCE SPECIFICATION FOR HIGH DENSITY INTERCONNECT (HDI) LAYERS OR BOARDS

FOREWORD

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IEC-PAS 62293 was submitted by the IPC (The Institute for Interconnecting and Packaging Electronic Circuits) and has been processed by IEC technical committee 91: Electronics assembly technology.

The text of this PAS is based on the following document:	This PAS was approved for publication by the P-members of the committee concerned as indicated in the following document:
Draft PAS	**Report on voting**
91/248/PAS	91/269/RVD

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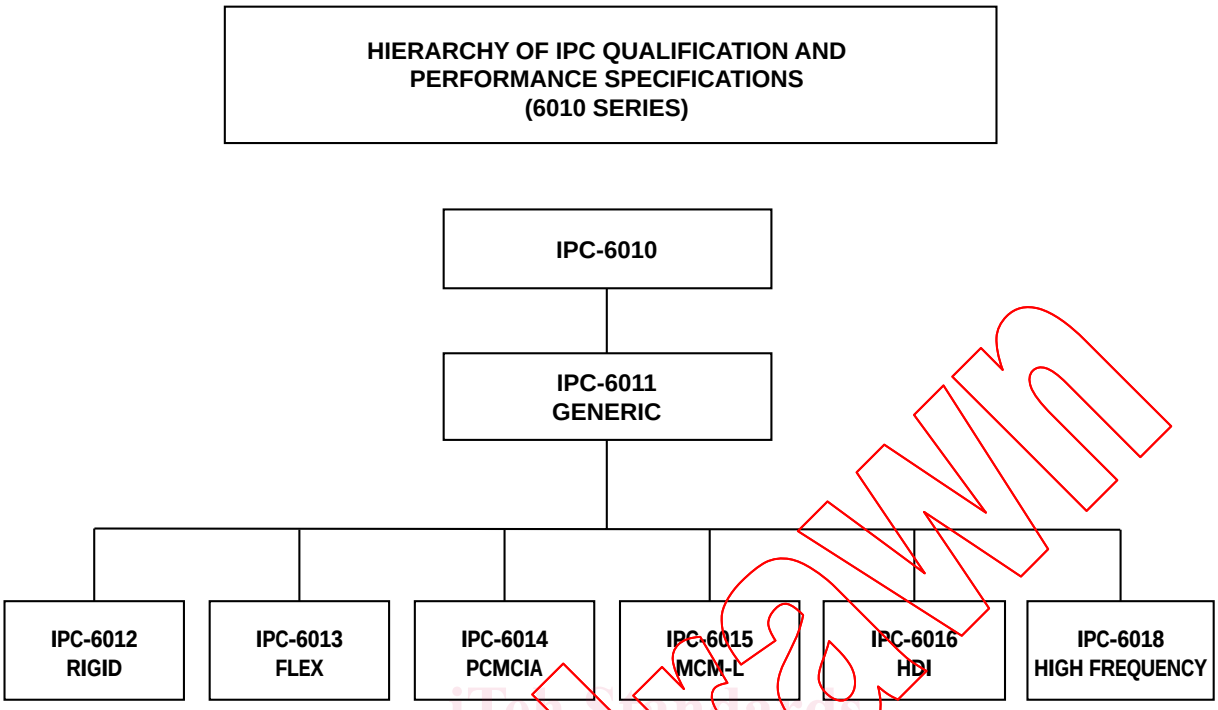

FOREWORD

This specification is intended to provide information on the detailed performance criteria of High Density Interconnect layers only. The information contained herein supplements the generic requirements, identified in IPC-6011, as well as requirements relating to the core construction, identified in the sectionals: IPC-6012 (rigid), IPC-6013 (flex), IPC-6015 (MCM-L) or IPC-6018 (microwave). This document would be specified for and apply only to the added HDI features. The HDI layer should not modify most (if any) of the criteria set forth in the specification for the core construction. When used together, these documents should lead both manufacturer and customer to consistent terms of acceptability. If the HDI board does not employ a core construction, the customer should decide and specify which sectional performance specification should be used for evaluating criteria that is not covered in this document.

Within this document there are a number of performance criteria that are application dependent. These criteria are listed ''slash sheets'' in the back of the document that detail performance requirements based upon application. A blank slash sheet is also included to define needed requirements (agreed to by manufacturer and customer) for applications not currently covered.

NOTE: IPC-6016 was developed with consideration to HDI layers that use modified ''conventional'' plated-through hole processes and chemistries. The industry does not yet have enough experience to develop performance standards for HDI layers formed by novel processes that are drastically different from ''conventional'' plated-through hole constructions (i.e., non-plated copper processes). As experiences are gathered, criteria for these processes will be added. In the meantime, the customer and manufacturer should work together to set the criteria for acceptance of product using the new technologies.

IPC's documentation strategy is to provide distinct documents that focus on specific aspects of electronic packaging issues. In this regard, document sets are used to provide the total information related to a particular electronic packaging topic. A document set is identified by a four digit number that ends in zero (0) (i.e., IPC-6010). The generic specification, the first document of the set, is supplemented by one or multiple sectional documents, each of which provide specific focus on one aspect of a topic or technology. IPC invites input on the effectiveness of the documentation and encourages user response through the ''Standard Improvement Form'' located at the back of each document.

Acknowledgment

Any Standard involving a complex technology draws material from a vast number of sources. While the principal members of the HDI Performance Subcommittee (D-43) are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC extend their gratitude.

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Qualification and Performance Specification for High Density Interconnect (HDI) Layers or Boards

1 SCOPE

This specification establishes the specific requirements for organic high-density interconnect (HDI) layers with microvia technology and the quality and reliability assurance requirements that must be met for their acquisition.

1.1 Purpose The requirements contained herein are intended to reflect the electrical, mechanical, and environmental properties unique to the HDI layer. It is NOT intended to specify overall requirements for the core, which are already documented in the sectional performance specifications: IPC-6012 (rigid), IPC-6013 (flex), IPC-6015 (MCM-L), or IPC-6018 (microwave).

1.2 Performance Classification This specification recognizes HDI layers or boards will be subject to variations in performance requirements based on end use. The acceptance criteria of HDI layers are organized into slash sheet categories (A, B, C, etc., see Appendix A), which reflect those typical end-use applications. Users of this document **shall** select a slash sheet category that most closely resembles their product and are encouraged to modify it as necessary.

1.3 Slash Sheet Categories

A. Chip Carrier

B. Hand Held (cell phones, pagers)

C. High Performance (avionics, military, medical)

D. Harsh Environment (automotive, space)

E. Portable (laptops, PDAs)

1.4 Documentation Hierarchy This document, combined with IPC-6011 and the applicable sectional performance specification(s) (IPC-6012, IPC-6013, IPC-6015 or IPC-6018), constitute a qualification and performance specification for HDI layers or boards.

2 APPLICABLE DOCUMENTS

The following specifications of the revision in effect at the time of order form a part of this document to the extent specified herein. If a conflict of requirements exists between IPC-6016 and the listed applicable documents, IPC-6016 **shall** take precedence.

2.1 IPC[1]

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-PC-90 General Requirements for Implementation of Statistical Process Control

IPC-FC-231 Flexible Base Dielectrics for Use in Flexible Printed Wiring

IPC-FC-232 Adhesive Coated Dielectric Films for Use as Cover Sheets for Flexible Printed Wiring and Flexible Binding Films

IPC-FC-241 Flexible Metal-Clad Dielectrics for Use in Fabrication of Flexible Printed Wiring

IPC-AI-642 User's Guidelines for Automated Inspection of Artwork, Innerlayers, and Unpopulated PWBs

IPC-TM-650 Test Methods Manual[2]

2.1.1 Microsectioning

2.1.1.2 Microsectioning—Semi or Automatic Technique Microsection Equipment (Alternate)

2.4.1 Adhesion, Tape Testing

2.4.8 Peel Strength of Metallic Clad Laminates

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2.6.7.2 Thermal Shock, Continuity and Microsection, Printed Boards

2.6.8 Thermal Stress, Plated-Through Holes

2.6.8.1 Thermal Stress, Laminate

2.6.20 Assessment of Plastic Surface Mount Components for Susceptibility to Moisture/Reflow Induced Damage

IPC-ET-652 Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards

IPC-CC-830 Qualification and Performance of Electrical Insulating Compound for Printed Board Assemblies

1. IPC, 2215 Sanders Road, Northbrook, IL 60062-6135
2. For convenience, applicable test methods are reprinted in the back of this standard. They represent the latest method in effect at the time of publication. Test methods may be updated independent of standard revision. Users should check the IPC website (www.ipc.org) for the most current test method available.

IPC-2221 Generic Standard on Printed Board Design

IPC-2226 Sectional Design Standard for Organic High Density Interconnect (HDI)

IPC-4101 Specification for Base Materials for Rigid and Multilayer Printed Boards

IPC-4104 Specification for High Density Interconnect (HDI) and Microvia Materials

IPC-6011 Generic Performance Specification for Printed Boards

IPC-6012 Qualification and Performance Specification for Rigid Printed Boards

IPC-6013 Qualification and Performance Specification for Flexible Printed Boards

IPC-6015 Qualification and Performance Specification for Organic Multichip Module (MCM-L) Mounting and Interconnecting Structures

IPC-6018 Microwave End Product Board Inspection and Test

IPC-7721 Repair and Modification of Printed Boards and Electronic Assemblies

2.2 Joint Industry Standards[1]

J-STD-003 Solderability Tests for Printed Boards

3 REQUIREMENTS

3.1 General Printed boards with HDI layers furnished under this specification **shall** meet or exceed all of the requirements of this document and applicable slash sheet or as modified by the procurement documentation.

3.1.1 Terms and Definitions The definition of terms used herein **shall** be as specified in IPC-T-50 or as listed in 3.1.1.1 through 3.1.1.4.

3.1.1.1 Target Land The land on which the microvia ends and makes connection.

3.1.1.2 Capture Land The land where the microvia starts, and varies in shape and size based on use (i.e., component mounting, via entrance conductor, etc.)

3.1.1.3 Microvia Processed/plated hole ≤ 0.15 mm diameter (this specification can also be used for layers or boards where vias are > 0.15 mm diameter).

3.1.1.4 Core A single-sided, double-sided or multilayer board or flex circuit that is used as a carrier for HDI layers and meets the requirements of one of the following performance specifications: IPC-6012, IPC-6013, IPC-6015 or IPC-6018.

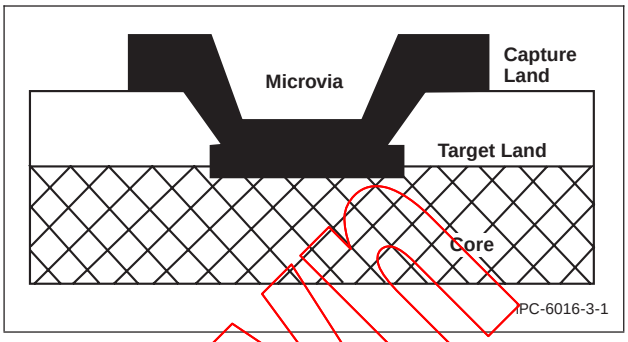

Figure 3-1 Typical Microvia Structure

3.2 Materials

3.2.1 Rigid Laminates Rigid reinforced laminates, clad and unclad, **shall** be as specified on the procurement documentation and **shall** be selected from IPC-4101 or IPC-4104. The type and metal thickness **shall** be as specified on the procurement documentation.

3.2.2 Flexible Films Flexible films, metal clad and unclad, **shall** be as specified on the procurement documentation and **shall** be selected from IPC-FC-231, IPC-FC-232 and IPC-FC-241. The type and metal thickness **shall** be as specified on the procurement documentation.

3.2.3 Bonding Materials Bonding materials **shall** be as specified on the procurement documentation and **shall** be selected from IPC-FC-232 and IPC-4101.

3.2.4 Other Dielectric and Conductive Materials Other materials **shall** be selected from IPC-4104 or as specified on the procurement documentation.

3.2.5 Metal Foils Metal foil materials **shall** be selected in accordance with the sectional performance specification for the applicable core board (i.e., IPC-6012 or IPC-6013).

3.2.6 Metallic Plating and Coatings The final circuit finish and other depositions **shall** be selected in accordance with and meet the requirements established in the applicable sectional performance specification (i.e., IPC-6012, IPC-6013, etc.). The minimum thickness of plated copper in the microvia **shall** be 10 µm. The minimum thickness of conductive material in microvias, which are formed and made conductive by a process that is significantly different from conventional plated-through hole constructions (i.e., non-plated copper processes), **shall** be as specified on the procurement documentation.

3.2.7 Solder Resist Solder resist material **shall** be selected in accordance with the applicable sectional performance specification (i.e., IPC-6012, IPC-6013, etc.).

3.2.8 Marking Inks Marking inks **shall** be selected in accordance with the applicable sectional performance specification (i.e., IPC-6012, IPC-6013, etc.).

3.2.9 Hole Fill Material When required, the material used for hole fill **shall** be selected from IPC-4104 or as specified on the procurement documentation. Hole fill material **shall** provide a planar surface and survive performance testing as the product requires without lifting or cracking the dielectric layer.

3.3 Visual Examination Finished boards using HDI layers **shall** be examined in accordance with the following procedure. They **shall** be of uniform quality and **shall** conform to 3.3.1 through 3.3.7.

Visual examination of the circuits for applicable dimensional or workmanship attributes **shall** be conducted at 30X minimum.

3.3.1 Edges Nicks or halos on finished board edges **shall** be acceptable provided the penetration does not bridge adjacent conductors or reduce the spacing requirements below the minimum specified on the procurement documentation. Nonconductive burrs along the edges of the finished board **shall** be acceptable.

3.3.2 Surface Dielectric Imperfections Pits or surface voids are acceptable provided they do not bridge conductors or reduce the spacing requirements below the minimum specified on the procurement documentation.

Scratches, dents, or tool marks are acceptable provided they do not penetrate to a depth that reduces the dielectric thickness below the minimum specified on the procurement documentation.

3.3.3 Lifted Lands The finished HDI layer or board **shall not** exhibit any lifted lands.

3.3.4 Marking Markings **shall** be in accordance with the applicable sectional performance specification (i.e., IPC-6012, IPC-6013, etc.).

3.3.5 Solderability Solderability of surfaces **shall** be in accordance with the applicable sectional performance specification (i.e., IPC-6012, IPC-6013, etc.).

3.3.6 Adhesion

3.3.6.1 Metal to Metal Adhesion The adhesion of the plating **shall** be tested in accordance with IPC-TM-650, Method 2.4.1, using a strip of pressure sensitive tape applied to the surface and removed by manual force applied perpendicular to the circuit pattern.

There **shall** be no evidence of any portion of the plating or the conductor pattern being removed, as shown by particles of the plating or pattern adhering to the tape. If overhanging metal breaks off (sliver) and adheres to the tape, this is not evidence of plating adhesion failure.

3.3.6.2 Metal to Dielectric Adhesion Peel strength testing **shall** be performed in accordance with IPC-TM-650, Method 2.4.8, if not supplied in the laminate certification. Type and frequency of test **shall** be specified on the procurement documentation. Peel strength **shall** meet the value specified on the applicable slash sheet.

3.3.6.3 Dielectric to Core Adhesion Thermal stress testing **shall** be performed in accordance with IPC-TM-650, Method 2.6.8.1. There **shall** be no evidence of delamination or blistering.

3.3.7 Workmanship HDI layers or boards **shall** be processed in such a manner as to be uniform in quality and show no visual evidence of dirt, foreign matter, oil, fingerprints, flux residue, and other contaminants that affect life, ability to assemble, and serviceability. Darkened appearance in non-plated holes, which is seen when the nonmetallic semi-conductive coating is used, is not foreign matter and does not affect life or function.

HDI layers or boards **shall** be free of defects in excess of those allowed in this specification. There **shall** be no evidence of any lifting or separation of platings from the surface of the conductive pattern, or of the conductor from the base laminate in excess of that allowed. There **shall** be no loose plating slivers on the surface of the HDI layer or board.

3.4 Dimensional Requirements All dimensional characteristics **shall** be as specified on the procurement documentation.

The accuracy, repeatability, and reproducibility of the equipment used to verify the characteristics of HDI layers or boards should be 10% or less of the tolerance range of the dimensions being verified. A measurement system evaluation **shall** be performed on each gauging system (see IPC-9191).

Automated inspection technology is allowed provided it meets requirements for repeatability (see IPC-AI-642).

3.4.1 Hole Pattern Accuracy The accuracy of the hole pattern on the HDI layer or board **shall** be as specified on the appropriate specification slash sheet.

3.4.2 Registration (Internal)

3.4.2.1 Microvia to Target Land Breakout at the target land is allowed up to 180°. Breakout, if it occurs, **shall**

neither reduce the intended contact area (at the target land) below that specified on the applicable slash sheet nor reduce the minimum electrical spacing below that specified on the procurement documentation. Registration measurements at the target land may (at the suppliers option) be determined during microsection evaluation (see 3.6) or by another method as agreed upon between supplier and user.

Note: If using an ablation-type process, tangency may be required as a minimum (due to potential reduction in dielectric separation).

3.4.2.2 Plated-Through Holes Internal registration for plated-through holes **shall** be in accordance with the applicable sectional performance specification (i.e., IPC-6012, IPC-6013, etc.).

3.4.3 Annular Ring (External)

3.4.3.1 Capture Land to Microvia Capture lands **shall** have tangency at a minimum. Breakout is not allowed, unless the design and procurement documentation specify (i.e., landless microvia). See Figure 3-2.

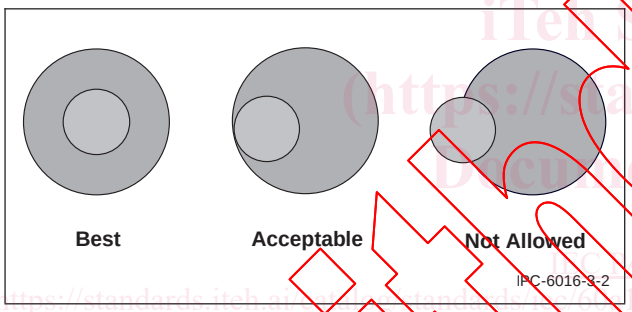

Figure 3-2 Capture Land Registration

3.4.3.2 Plated-Through Holes External annular ring for plated-through holes **shall** be in accordance with the applicable sectional performance specification (i.e., IPC-6012, IPC-6013, etc.).

3.4.4 Bow and Twist Bow, twist, or any combination thereof, **shall** be as specified in the applicable slash sheet and tested in accordance with IPC-TM-650, Method 2.4.22.

3.5 Conductor Definition All conductive surfaces on HDI layers or boards including conductors, lands and planes **shall** meet the visual and dimensional requirements of 3.5.1 through 3.5.3. Unless otherwise noted, visual examination of the circuits for applicable dimensional or workmanship attributes **shall** be conducted at 30X minimum. Other magnifications may be required by procurement documentation or specification. AOI inspection methods are permitted.

3.5.1 Conductor Width Unless otherwise specified on the procurement documentation, reductions **shall not** reduce the conductor width by more than that allowed on the respective slash sheet.

3.5.2 Conductor Spacing Unless otherwise specified on the procurement documentation, reductions **shall not** reduce the conductor spacing by more than that allowed on the applicable slash sheet.

3.5.3 Conductive Surfaces

3.5.3.1 Nicks and Pinholes in Ground or Voltage Planes For nicks and pinholes in ground or voltage planes, the maximum size allowed **shall** be 150 µm for Class 2 and 3, with no more than two per side per 25 mm x 25 mm.

3.5.3.2 Surface Mount Lands (Area for attachment such as solder, TAB, conductive adhesive) Defects such as nicks, dents, and pinholes along the edge of the land (length or width) **shall not** exceed that identified in the respective slash sheets.

3.5.3.3 Wire Bond Surface Unless otherwise defined on the procurement documentation, the bond site area **shall** be free of defects such as nicks, scratches, dents, bumps, pits, and pinholes. Other requirements (i.e., surface smoothness, hardness, etc.) **shall** be as defined between user and supplier.

3.5.3.3.1 Gold Plating Surface Wire bonding lands (gold plating surfaces) **shall** be free of any exposed nickel or copper.

3.5.3.3.2 Test Probe Dents Dents caused by test probes are acceptable when the bondable finish is not pierced and they do not violate wire bond adhesion requirements. Dents **shall** be no greater than 10 µm in diameter when examined under 10X magnification.

3.5.3.3.3 Surface Contaminants Wire bond surfaces **shall** be free of any contaminants, dirt, dust, foreign matter, and discolorations.

3.5.3.3.4 Wire Bond Adhesion Plated bonding area **shall** be evaluated in accordance with IPC-TM-650, Method 2.4.42.3, and capable of meeting the requirements of Table 3-1 without incurring any of the following situations:

a) Failure in bond (interface between wire and metallization) at substrate.

b) Separation of metallization layer on the land area.

c) Land is lifted from substrate.

3.5.3.4 Edge Board Connector Lands Edge board connector lands **shall** be in accordance with the applicable sectional performance specification (i.e., IPC-6012, IPC-6013, etc.).

Table 3-1 Wire Bond Adhesion Requirements

Test Condition	Wire composition and diameter	Minimum bond strength (grams force)
C or D	AL 18 AU 18	1.5 2.0
C or D	AL 25 AU 25	2.5 3.0
C or D	AL 32 AU 32	3.0 4.0
C or D	AL 33 AU 33	3.0 4.0
C or D	AL 38 AL 38	4.0 5.0
C or D	AL 76 AU 76	12.0 15.0

3.5.3.5 Conductor Edge Integrity Conductor edges **shall** have no evidence of slivers when tested in accordance IPC-TM-650, Method 2.4.1.

3.5.3.6 Nonwetting For conductive surfaces intended to be soldered, nonwetting is not permitted.

3.5.3.7 Final Finish Coverage Final finish coverage **shall** be in accordance with the applicable sectional performance specification (i.e., IPC-6012, IPC-6013, etc.).

3.5.3.8 Microvia in Land When microvias are employed as via-in-land technology, they **shall** be evaluated for acceptance as defined in the procurement documentation (i.e., coplanarity, solder wicking, entrapment).

3.6 Structural Integrity Structural integrity **shall** be evaluated on thermally-stressed test specimens or production boards using HDI.

Test specimens **shall** be representative of the part and agreed upon by user and supplier.

3.6.1 Thermal Stress Method Printed boards using HDI layers **shall** be preconditioned and tested in accordance with IPC-TM-650, Method 2.6.8, test condition B. The number of cycles **shall** be five (unless limited by the number of stress cycles acceptable for the core board) or as specified on the appropriate slash sheet.

3.6.2 Microsection Technique Following stress, HDI layers or boards **shall** be microsectioned by either of the two techniques outlined below or with another procedure agreed upon between user and supplier.

Microsectioning **shall** be accomplished per IPC-TM-650, either Method 2.1.1 or 2.1.1.2, on boards using HDI as agreed to between user and supplier. A minimum of three holes or vias **shall** be inspected in the vertical cross section. The grinding and polishing accuracy of the microsection **shall** be such that the viewing area of each of the three holes is within ± 10% of the diameter of the hole.

Microvias **shall** be examined for plating integrity and interconnection integrity at a magnification of 200X ± 5%. Referee examinations **shall** be accomplished at a magnification of 400X ± 5%. Each side of the hole **shall** be examined independently. Examination for laminate thickness, foil thickness, plating thickness, lay-up orientation, lamination, plating voids, and so forth, **shall** be accomplished at magnifications specified above.

Conventional plated-through holes **shall** be examined in accordance with the applicable sectional performance specification (i.e., IPC-6012, IPC-6013, etc.).

3.6.3 Microvia Integrity (after Thermal Stress)

3.6.3.1 Plating Integrity Plated-through holes, blind, and/or buried vias **shall** have no separation of plating layers, no plating cracks, and internal interconnections **shall** exhibit no separation or contamination between plated hole wall and internal layers. Any additional requirements **shall** be detailed on the procurement documentation.

3.6.3.2 Dielectric Integrity There **shall** be no dielectric voids that reduce dielectric separation (layer-to-layer or within the layer) below the minimum specified in the procurement documentation.

3.6.3.3 Copper Plating Thickness Based on microsection examination or the use of suitable electronic measuring equipment, copper plating thickness in the microvia **shall** be an absolute minimum of 10 µm, as specified on the respective slash sheet, or as stated in the procurement documentation. No voids are allowed.

3.6.3.4 Fused Tin-Lead Plating and Solder Coating Fused tin-lead plating and solder coating, if used on the HDI layer, **shall** meet the solderability requirements of J-STD-003. Solder or reflowed tin-lead coverage does not apply to vertical conductor edges.

3.6.3.5 Conductor Thickness Conductor thickness **shall** be greater than or equal to the minimum specified in the procurement documentation or ≥ 80% of the nominal specified in the procurement documentation for all non-via surfaces.

3.6.3.6 Dielectric Thickness The minimum dielectric thickness over circuitry **shall** be as specified in the procurement documentation.

3.6.3.7 Microvia Contact Area Microvia contact area, as defined by the interface between the microvia and the target land, **shall not** be reduced by more than that allowed on the applicable slash sheet. Any non-conductive residues on the surface of the target land **shall** be considered part of the reduced contact area. Contact area may be determined by another method as agreed upon between supplier and user.

3.6.4 Filled Vias Buried vias and/or buried microvias **shall** be filled and inspected in accordance with the procurement documentation. Blind vias on the external layers do not have any fill requirements.

3.6.5 Lifted Lands

3.6.5.1 Microvias The finished HDI board **shall not** exhibit any lifted microvia lands after thermal stress.

3.6.5.2 Plated-Through Holes Plated-through holes on the finished HDI board can exhibit lifted lands after thermal stress provided the visual criteria of 3.3.3 are met.

3.7 Other Tests Other test and requirements specific to HDI layers and boards may be required and should be called out in the applicable slash sheets.

3.7.1 Bond Strength, Unsupported Hole or Surface Mount Land A minimum of three unsupported holes or surface mount lands **shall** be tested in accordance with the following procedure. The surface mount land or land of an unsupported hole **shall** withstand 2 kg or kg/cm^2 whichever is less.

Bond strength **shall** be performed in accordance with IPC-TM-650, Method 2.4.21.1, for surface mount lands. For the unsupported hole lands, the soldering and tensile pull method are the same as in IPC-TM-650, Method 2.4.21.1. Calculations of land area of the unsupported hole do not include the area occupied by the hole.

3.8 Solder Resist (Solder Mask) Requirements Solder resist coverage **shall** be in accordance with the applicable sectional performance specification (i.e., IPC-6012, IPC-6013, etc.) and 3.8.1.

3.8.1 Solder Resist Coverage Encroachment of solder resist **shall not** reduce the design dimension of any conductive feature by more than 10% or by 100 µm, whichever is less. Encroachment of solder resist onto flip chip attachment sites **shall** be as specified on the procurement documentation.

3.9 Electrical Properties When tested as specified below, the HDI layers and boards **shall** meet the electrical requirements detailed in the following paragraphs.

3.9.1 Circuitry HDI layers and boards **shall** be tested in accordance to IPC-ET-652.

3.9.1.1 Continuity Printed boards using HDI or qualification test boards **shall** be tested in accordance with the following procedure. There **shall** be no circuits whose resistance exceeds that specified on the applicable slash sheet. The acceptability criteria for specialized conductors **shall** be specified on the procurement documentation.

The current passed through the conductors **shall not** exceed that specified in IPC-2221 and IPC-2226 for the smallest conductor in the circuit. For qualification, the test current **shall not** exceed one ampere. HDI boards with designed resistive patterns **shall** meet the resistance requirements specified on the procurement documentation.

Alternative test methods, agreed to by supplier and user, may be utilized to verify electrical integrity of HDI boards.

3.9.1.2 Isolation HDI layers or qualification test boards **shall** be tested in accordance with the following procedure. The isolation resistance between conductors **shall** be greater than specified on the applicable slash sheet.

The voltage applied between networks must be high enough to provide sufficient current resolution for the measurement. At the same time, it must be low enough to prevent arc-over between adjacent networks, which could induce defects within the product. The minimum applied test voltage **shall** be twice the maximum rated voltage of the board. If the maximum is not specified, the test voltage **shall** be 40 volts minimum.

3.9.2 Dielectric Withstanding Voltage Applicable coupons tested as outlined in the applicable slash sheets **shall** meet the requirements of those same slash sheets without flashover, sparkover, or breakdown between conductors or conductors and lands. The dielectric withstanding voltage test **shall** be performed in accordance with IPC-TM-650, Method 2.5.7. The dielectric withstanding voltage **shall** be applied between all common portions of each conductor pattern and adjacent common portions of each conductor pattern. The voltage **shall** be applied between conductor patterns of each layer and the electrically isolated pattern of each adjacent layer. Unless otherwise defined on the procurement documentation, test voltages **shall** appear on the appropriate specification sheets.

3.9.3 Insulation Resistance Test specimens **shall** be tested in accordance with the procedure outlined below. The insulation resistance **shall** be no less than that shown on the respective slash sheets.

Specimens **shall** be conditioned at 50° ± 5°C with no added humidity for a period of 24 hours. After cooling, the insulation resistance test **shall** be performed in accordance with the ambient temperature measurements specified in IPC-TM-650, Method 2.6.3.

3.10 Environmental HDI layers and boards **shall** meet the environmental requirements detailed in this section.

3.10.1 Moisture and Insulation Resistance Test coupons **shall** be tested in accordance with the procedure outlined below. The specimen **shall not** exhibit measling, blistering, or delamination in excess of that allowed in the