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Data requirements for semiconductor die -- Part 2: Vocabulary

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EUROPEAN SPECIFICATION
SPÉCIFICATION EUROPÉENNE
EUROPÄISCHE SPEZIFIKATION

ES 59008-2

September 1999

English version

Data requirements for semiconductor die
Part 2: Vocabulary

This European Specification was approved by CENELEC on 1999-06-29.

CENELEC members are required to announce the existence of this ES in the same way as for an EN and to make the ES available promptly at national level in an appropriate form. It is permissible to keep conflicting national standards in force.

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CENELEC
European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

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Foreword

This European Specification has been prepared by the CENELEC BTTF 97-1, Known good die.

It was submitted to the vote during the meeting of BTTF 97-1 and approved by CENELEC as ES 59008-2 on 1999-06-29.

The following dates was fixed:

- latest date by which the existence of the ES has to be announced at national level (doa) 1999-11-01

The structure of this European Specification is as follows.

ES 59008 Data requirements for semiconductor die
- Part 1 General requirements
- Part 2 Vocabulary
- Part 3 Mechanical, material and connectivity requirements
- Part 4 Specific requirements and recommendations
  - Part 4-1: Test and quality
  - Part 4-2: Handling and storage
  - Part 4-3: Thermal
  - Part 4-4: Electrical simulation
- Part 5 Particular requirements and recommendations for die types
  - Part 5-1: Bare die
  - Part 5-2: Bare die with added connection structures
  - Part 5-3: Minimally-packaged die
- Part 6 Exchange data formats and data dictionary
  - Part 6-1: Data exchange - DDX file format
  - Part 6-2: Data dictionary

Introduction

This European Specification has been developed so that the selection of unpackaged and minimally-packaged semiconductor die, with or without connection structures, can be carried out in a constructive way so that the designer and procurer of the components can save both design and procurement time.

It is a data specification which defines the requirements for :

- product identity
- product data
- die mechanical information
- test, quality and reliability information
- handling, storage and mounting information
- thermal data and electrical simulation data.

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This document was prepared by CENELEC Task Force CLC/BTTF 97-1 Known Good Die. Other organisations that helped prepare it were: the ESPRIT GOOD-DIE projects, EECA, Sematech, DPC and EIAJ.

The specification was derived from the work carried out in the ESPRIT 4th Framework project GOOD-DIE. This project was set up to develop a database for the selection of unpackaged and minimally-packaged semiconductor die, with or without connection structures, and for the downloading of information to CAD design stations to facilitate the layout and simulation of MCMs and hybrid circuits. During the early part of the GOOD-DIE project the need was identified for a standard way of presenting information for the selection and procurement of these components.

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1 Scope

This series of European Specifications specifies requirements for the exchange of data pertaining to bare semiconductor die, with or without connection structures, and minimally-packaged semiconductor die.

This Specification also gives recommendations for general industry good practice in the use of bare die, with or without connection structures, and minimally-packaged die.

ES 59008-2 specifies the vocabulary and definitions which are used throughout other parts of the Specification. It should be read in conjunction with ES 59008-1: General requirements.

2 Normative references

The following standards contain provisions which, through reference in this text, constitute provisions of this part of ES 59008.

ES 59008-1, *Data requirements for semiconductor die -- Part 1: General requirements*

ISO 8879, *The SGML Standard*

IEC 60050, *International Electrotechnical Vocabulary*

ISO/IEC 10303, *Industrial Automation Systems - Product Data Representation and Exchange (STEP)*

EN 100015-1, *Basic Specification: Protection of electrostatic sensitive devices Part 1: General requirements*

EDIF 2 0 0, *Electronic Design Interchange Format version 2 0 0*

EDIF 3 0 0, *Electronic Design Interchange Format version 3 0 0*

EDIF 4 0 0, *Electronic Design Interchange Format version 4 0 0*

IEEE 1149.1, *Standard Test Access Port and Boundary Scan Architecture*

IEEE 1364, *Verilog*

3 Definitions

For the purpose of this Specification, the following terms shall have the meanings given. All terms defined here are in addition to relevant terms which are defined in IEC 60050, International Electrotechnical Vocabulary.

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3.1 General terminology

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3.1.1
anti-static
generally referring to any material having the property of being relatively incapable of generating a static charge from frictive energy. Can also be used to describe electrostatic conductive and electrostatic dissipative materials where their use is to prevent the build up of an electrostatic charge. For further information, refer to EN 100015-1.

3.1.2
bare die
unpackaged discrete semiconductor or integrated circuit with bond pads on the upper surface suitable for interconnection to the substrate or package by wire bonding or soldered wiring

NOTE Typically these can be die that have had solder or other metallic bumps added to the metallised pads on the die in the form of peripheral bumps or arrays (also known as flip chip) or die that have had fine leads attached to the metallised pads on the die known as TAB.

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3.1.3
bare die with connection structures
unpackaged die that have had added bumps or other terminations to interconnect for electrical attachment

3.1.4
chip
common parlance for die

3.1.5
COB
Chip-On-Board. A mounting and attach technology where the die is mounted onto a substrate, often a PCB

3.1.6
CSP
Chip Scale Package. Generic term for packaging technologies that result in a packaged part that is only marginally larger than the internal die

3.1.7
die (singular or plural)
piece(s) of semiconductor wafer which constitute a discrete semiconductor or whole integrated circuit

3.1.8
die device
a bare die, with or without connection structures, or a minimally-packaged die

3.1.9
discrete (discrete semiconductor)
single 2-, 3- or 4- terminal semiconductor device

3.1.10
hybrid(hybrid circuit)
module or encapsulated sub-assembly that comprises semiconductor die and printed or otherwise attached passive components. Also see MCM.

3.1.11
IC
Integrated Circuit (semiconductor). A collection of transistors and other components fabricated on a semiconductor material that creates an electrical function or sub-function

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3.1.12
KGD
Known Good Die. A qualification of a semiconductor die which indicates that the die has been tested to a specified or determined level of quality or “goodness”

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NOTE A commonly accepted definition of KGD is a die that has been tested to quality levels which are of the same order as those applicable to the equivalent packaged parts.

3.1.13
MCM
Multi-Chip Module. A module or small sub-assembly that contains two or more die and/or MPDs. Also see hybrid

3.1.14
MCM-C
MCM using interconnections on a ceramic substrate

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3.1.15
MCM-D
MCM using interconnections on a deposited-film substrate

3.1.16
MCM-L
MCM using interconnections on a laminated substrate

3.1.17
minimally-packaged die (MPD)
die that have had some exterior packaging media and interconnection structure added for protection and ease of handling

NOTE These are commonly known as Chip Scale Packages (CSPs), covering such package styles as SON, µBGA etc. This is a generic term for a packaged device that is only slightly larger than the die itself, where the area of the package is typically not greater than 1,2 times the area of the bare die.

3.1.18
packaging
package, interconnect or encapsulation technique

NOTE : The use of "packaging" as a participle (e.g. "When packaging ICs into dual-in-line packages ...") is deprecated.

3.1.19
packing
material which is used to protect electronic items from mechanical, environmental and electrical damage during transportation and storage. It is discarded prior to the incorporation of the item into its end application

3.1.20
pin-in-hole
A common term used to express an assembly and PCB technology whereby components are attached by and connected to pins or leads that are mounted through holes in the PCB

3.1.21
SME
Small or Medium sized Enterprise. A company of less than a defined size which is eligible for certain favourable treatment from National and European governments

3.1.22
SMT
Surface Mount Technology. An assembly and PCB technology requiring the components to be mounted on the surface of a PCB, without the need of holes to align and connect to the component pins

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3.1.23
substrate
a) term used to describe the base element consisting of one or more layers of material upon which die are mounted
b) the bulk and/or base material of the die itself

3.1.24
terminal
a geometric shape to which an electrical connection may be made

NOTE For bare die without external connections, the terminal takes the form of a metallised pad on the surface of the die. For bumped die the terminal is in the form of additional conducting material placed on a pad whilst for die with lead frame the terminal is in the form of a conductor connected to the pad and extending from the die. For minimally-packaged die the form of the terminal depends on the package style. On a substrate or PCB on which die are mounted the terminal is a connection land, hole or via.

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3.1.25
wafer
thin slice of semiconductor or other material, usually circular, upon which many die devices are made as part of the manufacturing process

3.2 Test terminology

3.2.1
absolute maximum ratings
the range of voltages, currents, temperatures, etc., beyond which a device may suffer degradation in performance or reliability, may cease functioning or may suffer irreversible damage

3.2.2
bond pull
test involving the pulling of the bond wires to destruction to determine the strength of the bonds

3.2.3
burn-in
time/temperature related process intended to prematurely age devices in order to uncover early failures

3.2.4
DUT
Device Under Test. The actual IC or semiconductor device that is currently undergoing electrical or environmental test

3.2.5
EPA
ESD Protected Area. An area or workplace that has protection against ESD (q.v.)

3.2.6
ESD
Electro-Static Discharge. Generally with reference to damage caused to semiconductor devices due to an ESD

3.2.7
ESDS
Electro-Static Discharge Sensitive device. A device with known sensitivity or susceptibility to ESD (q.v.)

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3.2.8
lot accept number
maximum number of devices which may fail a sample test without causing rejection of the lot

3.2.9
lot reject number
for a sample test, the number of failed devices which will cause lot rejection

3.2.10
LTPD
Lot Tolerance Percent Defective. A single lot sampling concept that statistically ensures rejection of 90% of all Lots having a greater percent defective than the specified LTPD

3.2.11
prober
machine intended to permit electrical connection to individual die on a wafer (q.v.)

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3.2.12
resistance to solvents
test which requires immersion of sample devices in such solvents as trichlorotrifluoroethane and methylene chloride, followed by brushing to determine the durability of unit marking

3.2.13
sampling plan
statistically derived set of sample sizes, accept numbers, and/or reject number which will confirm that a given Lot of materials meets established AQLs or LTPDs

3.2.14
stabilisation bake
placement of devices in a chamber at elevated temperature without electrical bias

3.2.15
temporary carrier
system of contacts, used to hold die during electrical test, which does not make permanent contact to the die, and which possibly can be re-used

3.2.16
testability
measure of whether an IC can be electrically tested economically in production

3.2.17
tester
generic term generally relating to an electronic apparatus designed and used for the purposes of testing and analysing electronic components, including integrated circuits

3.2.18
test vectors
series of test stimuli and expected responses applied to and received by either a simulator to a device model, or a tester to an actual device

3.3 Semiconductor terminology

3.3.1
bipolar
transistor fabrication technology, resulting in the creation of bipolar transistor devices

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3.3.2
MOS
Metal Oxide Silicon, a fabrication technology, resulting in the creation of FET devices

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3.3.3
NMOS
N-type Metal Oxide Silicon. A fabrication technology that results in the creation of NMOS FET devices

3.3.4
PMOS
P-type Metal Oxide Silicon. A fabrication technology that results in the creation of PMOS FET devices

3.3.5
CMOS
Complementary Metal Oxide Silicon. A fabrication technology, resulting in the creation of both NMOS and PMOS FET devices

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3.3.6
BiCMOS
transistor fabrication technology, resulting in the creation of both bipolar and CMOS devices

3.3.7
GaAs
Gallium Arsenide (GaAs) technology. A semiconductor material having higher performance speeds than silicon

3.3.8
micron
unit of length, 10^{-6} metre. Commonly used to describe the geometry of a process, the smallest viable dimension sustainable and practicable in that process

3.3.9
mil
unit of length, 10^{-3} inch. A non-preferred unit commonly used in describing the dimensions of a die

3.3.10
MPW
Multi-Project Wafer. A means of processing prototypes or low volume runs of different ASICs on the same wafer

3.3.11
SOI
Silicon On Insulator. A general term describing a fabrication technology that uses an insulating material as the bulk material instead of Silicon, which may be Sapphire (SOS)

NOTE It is generally implied that an SOI technology is also a CMOS technology.

3.3.12
SOS
Silicon On Sapphire. A specific fabrication technology that uses sapphire, a variety of corundum (Al_2O_3), as the bulk material instead of silicon

NOTE It is generally implied that an SOS technology is also a CMOS technology.

3.4 Semiconductor manufacturing & interconnection terminology

3.4.1
mask
a) originally referred to an optical overlay used in photo-etching during the process of semiconductor fabrication

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b) now used as a general term to refer to the major individual patterning stages that are used within the fabrication process. The complexity and cost of a process increases with an increase in the number of masks employed

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3.4.2
layer
loose topological term used in describing the process of semiconductor fabrication. A layer consists of a specific material and a semiconductor device consists of many layers

3.4.3
metal
metallic conducting layer, usually but not specifically aluminium

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3.4.4
metallisation run
lot of wafers metallised at the same time. Since the number of wafers accommodated by the evaporation (i.e. metallisation) chamber is frequently less than the number of wafers accommodated by a diffusion chamber, it is possible to have several metallisation runs which come from the same wafer run

3.4.5
via
conducting material placed in a void or hole in a non-conducting layer in order to connect two or more conducting layers together

3.4.6
poly
layer consisting of poly-crystalline silicon

3.4.7
glassivation
top layer(s) of transparent insulating material which covers the active circuit area including metallisation, except bond pads. Also see passivation

3.4.8
passivation
top or final processing and covering on a die, usually of semiconductor oxide or nitride, that protects and seals the active areas of the die from further external chemical or mechanical contamination. Bond pads require an opening in this passivation to allow electrical contact

3.4.9
passivation step
change in thickness of the passivation for metal-to-metal or metal-to-semiconductor interconnection by design, where passivation layers have been removed as a result of normal device processing

3.4.10
crazing
minute cracks in the glassivation

3.4.11
glob top
encapsulation performed by depositing an epoxy resin or similar material over a bonded or attached die

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3.4.12
contact window
opening that has been etched in the semiconductor oxide, nitride or other insulating layer, grown or deposited directly onto the die, so as to allow ohmic contact to the underlying semiconductor material

3.4.13
scribe line, scribe lane
area surrounding the die that is set aside on the wafer for the purposes of scribing and sawing the die from the wafer

3.4.14
die separation, dicing, sawing
the means by which individual die are cut from the wafer, commonly by a fine circular saw