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Data requirements for semiconductor die -- Part 4-4: Specific requirements and recommendations - Electrical simulation

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Ta slovenski standard je istoveten z: ES 59008-4-4:1999

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2003-01.Slovenski inštitut za standardizacijo. Razmnoževanje celote ali delov tega standarda ni dovoljeno.

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EUROPEAN SPECIFICATION

SPÉCIFICATION EUROPÉENNE

EUROPÄISCHE SPEZIFIKATION

ES 59008-4-4

November 1999

English version

Data requirements for semiconductor die
Part 4-4: Specific requirements and recommendations
Electrical simulation

This European Specification was approved by CENELEC on 1999-09-23.

CENELEC members are required to announce the existence of this ES in the same way as for an EN and to make the ES available promptly at national level in an appropriate form. It is permissible to keep conflicting national standards in force.

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CENELEC
European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B - 1050 Brussels

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Ref. No. ES 59008-4-4:1999 E

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Foreword

This European Specification has been prepared by the CENELEC BTTF 97-1, Known good die.

It was submitted to the vote during the meeting of BTTF 97-1 and approved by CENELEC as ES 59008-4-4 on 1999-09-23.

The following date was fixed:

- latest date by which the existence of the ES has to be announced at national level (doa) 2000-02-01

The structure of this European Specification is as follows.

ES 59008 Data requirements for semiconductor die
- Part 1 General requirements
- Part 2 Vocabulary
- Part 3 Mechanical, material and connectivity requirements
- Part 4 Specific requirements and recommendations
  - Part 4-1: Test and quality
  - Part 4-2: Handling and storage
  - Part 4-3: Thermal
  - Part 4-4: Electrical simulation
- Part 5 Particular requirements and recommendations for die types
  - Part 5-1: Bare die
  - Part 5-2: Bare die with added connection structures
  - Part 5-3: Minimally-packaged die
- Part 6 Exchange data formats and data dictionary
  - Part 6-1: Data exchange - DDX file format
  - Part 6-2: Data dictionary

Introduction

This European Specification has been developed to facilitate the selection of unpackaged and minimally-packaged semiconductor die, with or without connection structures in order to save both design and procurement time.

It is a data specification which defines the requirements for :

- product identity
- product data
- die mechanical information
- test, quality and reliability information
- handling, storage and mounting information
- thermal data and electrical simulation data.

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This document was prepared by CENELEC Task Force CLC/BTTF 97-1 Known Good Die. Other organisations that helped prepare it were: the ESPRIT GOOD-DIE projects, EECA, Sematech, DPC and EIAJ.

The specification was derived from the work carried out in the ESPRIT 4th Framework project GOOD-DIE. This project was set up to develop a database for the selection of unpackaged and minimally-packaged semiconductor die, with or without connection structures, and for the downloading of information to CAD design stations to facilitate the layout and simulation of MCMs and hybrid circuits. During the early part of the GOOD-DIE project the need was identified for a standard way of presenting information for the selection and procurement of these components.

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1 Scope

This series of European Specifications specifies requirements for the exchange of data pertaining to bare semiconductor die, with or without connection structures, and minimally packaged semiconductor die.

This Specification also gives recommendations for general industry good practice in the use of bare die, with or without connection structures, and minimally packaged die.

ES 59008-4-4 specifies the use of models to simulate the electrical behaviour and the correct functionality of electronic systems that include bare semiconductor die, with or without connection structures, and/or minimally packaged semiconductor die.

2 Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this European Specification. At the time of publication, the editions indicated were valid. All normative documents are subject to revision, and parties to agreements based on this European Specification are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below.

ES 59008-1, *Data requirements for semiconductor die -- General requirements*

ES 59008-2, *Data requirements for semiconductor die -- Vocabulary*

ES 59008-3, *Data requirements for semiconductor die -- Mechanical, material and connectivity requirements*

ISO 8601:1998, *Numerical date/time interchange format*

3 Definitions

For the purpose of this European Specification, the definitions as given in ES 59008-2 apply.

4 Requirements

This Part 4-4 of ES 59008 should be read in conjunction with ES 59008-1 and ES 59008-3.

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Requirements and recommendations provided in this part of the Specification apply to electrical simulation models used to perform the following simulations:

- analysis of the signal propagation within the electronic system;
- verification of the correct functionality of the electronic system,
- verification of the timing requirements,
- verification of the testability.

Background information on the use of electrical simulation models is provided in annex A.

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5 Conformity levels

When any data are supplied which claim conformity to this specification, the level of conformity shall be stated as follows:

Level 1: all data listed in **6.1** have been included.

Level 2: all data listed in **6.1**, **6.2** and/or **6.1** and **7.1** have been included.

Level 3: all data listed in **6.1, 6.2, 6.3** and/or **6.1, 6.3, 7.2** have been included.

6 Requirements for bare die

This clause covers the requirements for bare die. However, since not all requirements are applicable to all types of die, Table 1 summarises the requirements in the first three columns where the figure shows the level of the requirement for each die type.

6.1 Essential information

In order to claim conformity with any of the levels 1, 2 or 3 all the information covered by 6.1.1 to 6.1.8 shall be given as indicated by a figure 1 in the relevant column of Table 1.

Where a simulation model is provided, the following information shall be given:

6.1.1 Model file name

Name of the model file.

6.1.2 Creation date

Date of the creation of the model file, compliant with ISO 8601:1998.

6.1.3 Model description

Description of the model.

6.1.4 Model source

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Source of the model.

6.1.5 Simulator name

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Name of the simulator accepting the model file as a valid input.

6.1.6 Simulator version

Version of the simulator compatible with the given file.

6.1.7 Compliance level

Level of the simulator the model file complies to (e.g.: SPICE level 3).

6.1.8 Model scope

Scope of the model (e.g.: VHDL behavioural model).

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6.2 Desirable information

The information covered by this subclause is important and should be supplied if at all possible. In order to claim conformity with either level 2 or 3 all the information covered by 6.1.1 to 6.1.8 and 6.2.1 to 6.2.4 shall be given as indicated by a figure 1 or 2 in the relevant column of Table 1.

6.2.1 Input pad capacitance

The capacitance of each input pad of the device.

6.2.2 Output pad capacitance

The capacitance of each output pad of the device.

6.2.3 Power pad capacitance

The capacitance of each power pad of the device.

6.2.4 Ground pad capacitance

The capacitance of each ground pad of the device.

6.3 Optional information

The information covered by this subclause should be supplied whenever it is applicable and available. In order to claim conformity with level 3 all the information covered by 6.1.1 to 6.1.8, 6.2.1 to 6.2.4 and 6.3.1 to 6.3.4 shall be given as indicated by a figure 1, 2 or 3 in the relevant column of Table 1.

6.3.1 Input buffer

The electrical model of each input buffer type.

6.3.2 Output buffer

The electrical model of each output buffer type.

6.3.3 ESD protection

A description of the ESD protection circuitry, if any.

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6.3.4 Timing simulation model

The appropriate model(s) describing the component's behaviour in the time dimension.

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Examples of such models include:

- VITAL;
- VERILOG;
- IEEE 1029.1 Waveform and Vector Exchange Specification IEC 61691-3-4, Timing expression in VHDL.

NOTE The model should be provided as an electronic file, so that it can be directly used as input to the simulator.

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7 Requirements for bare die with added connection structures and for minimally packaged devices

Information as described in the following subclauses is required in addition to any relevant information as defined in clause 6. These additional requirements are shown in the last 3 columns of Table 1 where the figure shows the level of requirement for each item of information for bare die with added connection structures and minimally-packaged devices.

7.1 Desirable information

The information covered by this subclause is important and should be supplied if at all possible. In order to claim conformity with either level 2 or 3 all the information covered by 6.1.1 to 6.1.8; 6.2.1 to 6.2.4 and 7.1.1 to 7.1.6, as indicated by a figure 1 or 2 in the relevant column of Table 1, shall be given.

7.1.1 Package or redistribution trace resistance

The resistance of the internal traces of the package or of the redistribution traces, if any.

7.1.2 Package trace capacitance

The self and mutual capacitance of the internal traces of the package or of the redistribution traces, if any, in matrix form.

7.1.3 Package trace inductance

The self and mutual inductance of the internal traces of the package or of the redistribution traces, if any, in matrix form.

7.1.4 Terminal resistance

The resistance of the package terminal (bump, lead or ball).

7.1.5 Terminal capacitance

The self and mutual capacitance of the package terminal (bump, lead or ball), in matrix form.

7.1.6 Terminal inductance

The self and mutual inductance of the package terminal (bump, lead or ball), in matrix form.

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Table 1 — Summary of information requirements (normative)

Subclause	Parameter	Bare die	Bumped die	Die with lead frame	Minimally packaged die
6.1.1	Model file name	1	1	1	1
6.1.2	Creation date	1	1	1	1
6.1.3	Model description	1	1	1	1
6.1.4	Model source	1	1	1	1
6.1.5	Simulator name	1	1	1	1
6.1.6	Simulator version	1	1	1	1
6.1.7	Compliance level	1	1	1	1
6.1.8	Model scope	1	1	1	1
6.2.1	Input pad capacitance	2	2	2	2
6.2.2	Output pad capacitance	2	2	2	2
6.2.3	Power pad capacitance	2	2	2	2
6.2.4	Ground pad capacitance	2	2	2	2
6.3.1	Input buffer model	3	3	3	3
6.3.2	Output buffer model	3	3	3	3
6.3.3	ESD protection model	3	3	3	3
6.3.4	Timing simulation model	3	3	3	3
7.1.1	Package trace resistance		2	2	2
7.1.2	Package trace capacitance		2	2	2
7.1.3	Package trace inductance		2	2	2
7.1.4	Terminal resistance		2	2	2
7.1.5	Terminal capacitance		2	2	2
7.1.6	Terminal inductance		2	2	2

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