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МЕЖДУНАРОДНАЯ ОРГАНИЗАЦИЯ ПО СТАНДАРТИЗАЦИИ

Fluid power systems and components — Fluid logic circuits —

Part 1: Symbols for binary logic and related functions

Transmissions hydrauliques et pneumatiques — Logique par les fluides —

Partie 1: Symboles pour fonctions logiques binaires et connexes

Reference number
ISO 5784-1 : 1988 (E)

Foreword

ISO (the International Organization for Standardization) is a worldwide federation of national standards bodies (ISO member bodies). The work of preparing International Standards is normally carried out through ISO technical committees. Each member body interested in a subject for which a technical committee has been established has the right to be represented on that committee. International organizations, governmental and non-governmental, in liaison with ISO, also take part in the work. ISO collaborates closely with the International Electrotechnical Commission (IEC) on all matters of electrotechnical standardization.

Draft International Standards adopted by the technical committees are circulated to the member bodies for approval before their acceptance as International Standards by the ISO Council. They are approved in accordance with ISO procedures requiring at least 75 % approval by the member bodies voting.

International Standard ISO 5784-1 was prepared by Technical Committee ISO/TC 131, *Fluid power systems.*

Users should note that all International Standards undergo revision from time to time and that any reference made herein to any other International Standard implies its latest edition, unless otherwise stated.

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Contents

Fluid power systems and components — Fluid logic circuits —

Part 1:
Symbols for binary logic and related functions

0 Introduction

0.1 In fluid power systems, power is transmitted and controlled through a fluid (liquid or gas) under pressure within a circuit.

Graphical symbols are used in diagrams of hydraulic and pneumatic equipment and accessories for fluid power transmission.

0.2 ISO 5784 on symbols for fluid logic circuits comprises the following three parts:

Part 1: Symbols for binary logic and related functions.

Part 2: Symbols for supply and exhausts as related to logic symbols.

Part 3: Symbols for logic sequencers and related functions.

1 Scope and field of application

This part of ISO 5784 defines graphical symbols for binary logic and related functions and gives some rules concerning their use in circuit diagrams.

Symbols given in this part of ISO 5784 shall be used for all documents and circuit diagrams concerning logic and related functions for data processing, especially in fluid logic circuits.

2 References

ISO 1219, *Fluid power systems and components — Graphic symbols.* [1)]

ISO 5598, *Fluid power systems and components — Vocabulary.*

IEC Publication 617-12, *Graphical symbols for diagrams — Part 12: Binary logic elements.*

3 Definitions

For the purposes of this part of ISO 5784, the definitions given in ISO 5598 apply.

4 General

The two values of a binary digital variable are assigned logic states which may be represented by any two arbitrary symbols. It has become usual practice to use the symbols 0 and 1 for this purpose.

In fluid logic applications the logic states represent two different pressure levels. Normally the higher pressure level represents the logic state 1 (positive logic).

5 Composition of the symbols and rules for their use

5.1 General rules

The following rules are applicable to all the symbols presented in this part of ISO 5784.

The form A symbols in this part of ISO 5784 are in accordance with IEC Publication 617-12 and are to be preferred; the form B symbols, although currently used, are not preferred for future use.

This part of ISO 5784 gives the most currently used logic functions and shows also how to apply these rules. Subject to these rules any other symbols may be developed.

NOTES

1 The following examples make use of the letters X, Y, Z, S... a, b, c, etc., to define logic equations. The convention is used for convenience only and should not be taken as part of the requirements laid down in this part of ISO 5784.

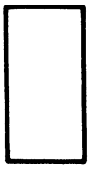
2 The addition of truth tables and Boolean equations are meant as explanations; they are not part of the requirements laid down in this part of ISO 5784.

1) The cross-reference to item 8.1.1 in ISO 1219 applies to the first edition published in 1976.

5.2 Composition of the symbols

A symbol comprises the following parts:

a) An outline

Code number	Graphical symbol Form A	Description	Graphical symbol Form B [1]
5 200-05/1		Logic element: General symbol The choice of form A or B is left to the user but reference shall be made to 5.1. However in any given circuit diagram, only one form (either A or B) shall be used. NOTE — The aspect ratio is arbitrary.	
5 200-06/1			

b) A qualifying symbol denoting the logic function

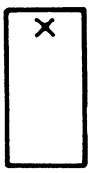
This is a symbol which specifies the required logic operation. In certain cases, this symbol may be accompanied by numerical values necessary to define the function of the element.

This symbol and/or these numerical values are drawn usually inside the outline.

c) Indicators for inputs and outputs

Each of these indicators is related to the input or the output against which it appears. The indicators shall be positioned as indicated in clause 5.3.

5.3 Position of the qualifying symbol for the logic function

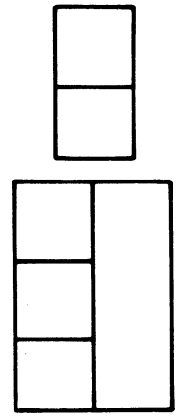
Code number	Graphical symbol Form A	Description	Graphical symbol Form B [1]
5 300-05/1		The qualifying symbol for the function or the numerical values is (are) located in the top centre of the outline or in the centre (form A) or in the centre of the outline (form B).	

5.4 Additional information

Any kind of additional information, e.g. type, function or location of the element, shall be written outside the outline of the symbol, below or following the qualifying symbol.

1) This form is not preferred for future use (see 5.1).

5.5 Combination of symbols

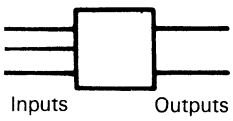
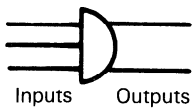
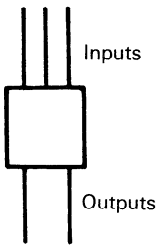
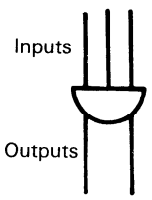
Code number	Graphical symbol Form A	Description	Graphical symbol Form B [1]
5 500-05/1 5 500-06/1		Separated symbols shall be used in logic circuit diagrams; however, to reduce space required on the diagram, symbols for basic operations may be joined together but the following rules shall then be complied with: a) there is no logic connection when the half-circles are tangents (form B) or the common line to two symbols is in the direction of information flow (form A); b) there is single logic connection, without logic inversion, when the common line to two symbols is perpendicular to the direction of information flow.	

5.6 Direction of information flow

Code number	Graphical symbol Forms A and B	Description
5 600-05/1		In principle, the information flow is directed from left to right or from top to bottom. If this is not possible and the direction of information flow is not obvious, lines carrying information with arrow heads may be marked which shall not be located adjacent to the logic symbol at inputs and outputs.

5.7 Inputs and outputs

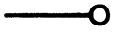
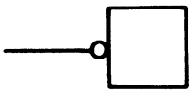
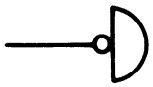
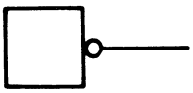
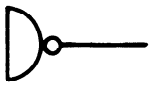
5.7.1 Input and output connections to the symbol

Code number	Graphical symbol Form A	Description	Graphical symbol Form B [1]
5 710-05/1		The inputs and outputs are located on opposite sides of the symbol.	
5 710-06/1		A logic symbol may have any number of inputs and outputs providing the symbol definition requirements are met.	

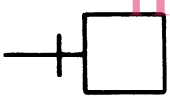
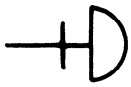
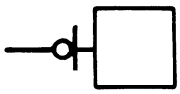
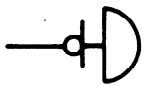
1) This form is not preferred for future use (see 5.1).

5.7.2 Negation

The state of the logic variable at an input or output is reversed if the logic negation indicator is applied.

Code number	Graphical symbol Form A	Description	Graphical symbol Form B [1]
5 720-05/1		Logic negation indicator (complement)	
5 720-10/1		Negated input	
5 720-15/1		Negated output NOTE — The line of input or output may be drawn through the circle.	

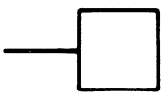
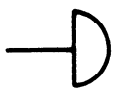
5.7.3 Inhibiting and negated inhibiting inputs

Code number	Graphical symbol Form A	Description	Graphical symbol Form B [1]
5 730-05/1		Inhibiting input: a) an inhibiting input of a digital element standing at its defined 1-state prevents the output variable of that element from standing at its defined 1-state (or its 0-state if the output is negated) whatever the value of the other input variables; b) when the inhibiting input stands at its 0-state the qualifying symbol of the element applies to those inputs which are neither inhibiting inputs nor negated inhibiting inputs.	
5 730-10/1		Negated inhibiting input: a) a negated inhibiting input of a digital element standing at its 0-state prevents the output variable of that element from standing at its defined 1-state (or its 0-state if the output is negated) whatever the value of the other input variables; b) when the negated inhibiting input stands at its defined 1-state the qualifying symbol of the element applies to those inputs which are neither inhibiting inputs nor negated inhibiting inputs.	

5.7.4 Static and dynamic inputs

5.7.4.1 Static input

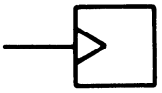
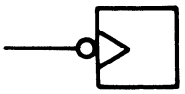
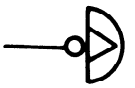
A static input is one such that 1-state is defined as the presence of a particular digital level, and the 0-state as the presence of the other logic level.

Code number	Graphical symbol Form A	Description	Graphical symbol Form B [1]
5 741-05/1		Static input	

1) This form is not preferred for future use (see 5.1).

5.7.4.2 Dynamic input

A dynamic input is one such that the 1-state is defined as the transition from a particular digital level to the other digital level and not by the presence of one of these logic levels.

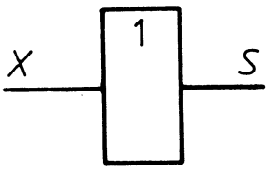
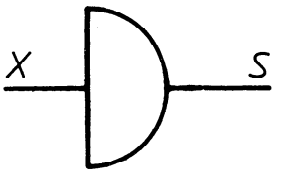
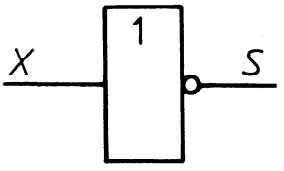
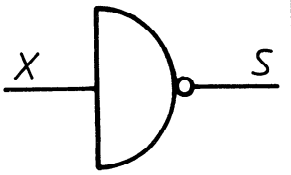
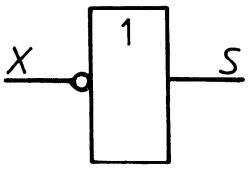
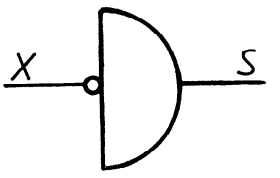
Code number	Graphical symbol Form A	Description	Graphical symbol Form B[1]
5 742-05/1		Dynamic input for which the dynamic 1-state is defined by the transition from the static 0-state to the static 1-state.	
5 742-10/1		Dynamic input for which the dynamic 1-state is defined by the transition from the static 1-state to the static 0-state.	

6 Combinative functions

6.1 Basic rule for the composition of the symbol

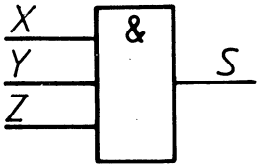
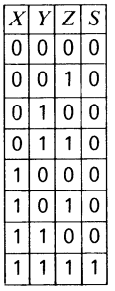
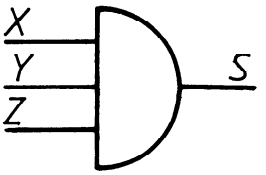
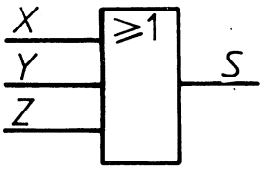
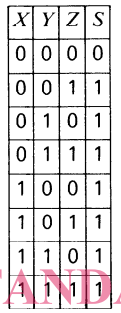
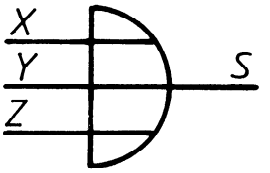
The qualifying symbol indicates the number of inputs which shall necessarily assume the defined 1-state so as to cause the output to assume its defined 1-state provided that the output is not negated.

6.2 Elementary combinative functions

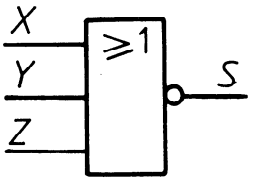
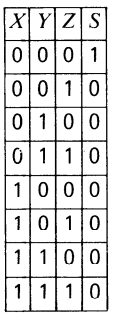
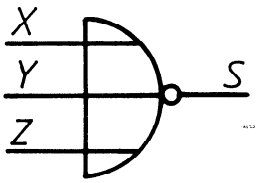
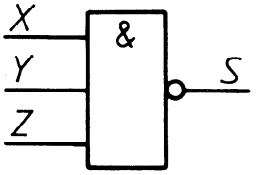
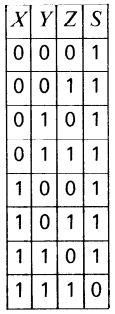
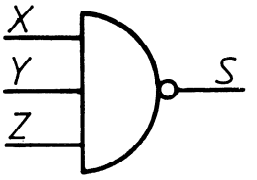
Code number	Graphical symbol Form A	Description	Graphical symbol Form B[1]
6 200-05/1		YES function X | S 0 | 0 1 | 1 The output will stand at its defined 1-state if, and only if, the input stands at its defined 1-state. $S = X$	
6 200-10/1		NO function The output will stand at its 0-state if, and only if, the input stands at its defined 1-state.	
6 200-11/1		X | S 0 | 1 1 | 0 $S = \overline{X}$	

1) This form is not preferred for future use (see 5.1).

6.2 Elementary combinative functions (*concluded*)

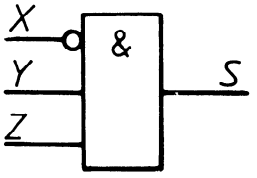
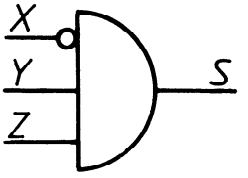
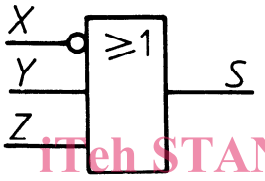
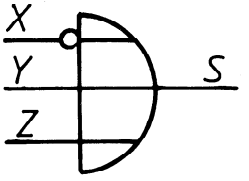
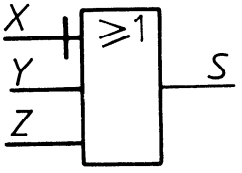
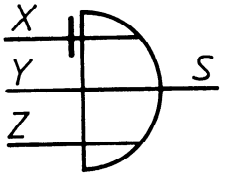
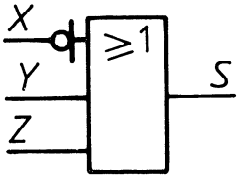
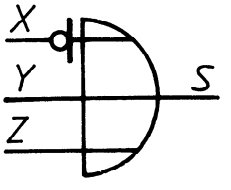
Code number	Graphical symbol Form A	Description	Graphical symbol Form B [1]
6 200-15/1		 AND function The output will stand at its defined 1-state if, and only if, all of the inputs stand at their defined 1-states. $S = X\,Y\,Z$	
6 200-20/1		 OR function The output will stand at its defined 1-state if, and only if, one or more of its inputs stand at their defined 1-states. $S = X + Y + Z$ NOTE – "≥1" may be replaced by "1" if no ambiguity arises.	

6.3 Derived combinative functions — Examples

Code number	Graphical symbol Form A	Description	Graphical symbol Form B [1]
6 300-05/1		 NOR function, i.e. OR function with negated output The output will stand at its 0-state if, and only if, at least one input stands at its defined 1-state. $S = \overline{X + Y + Z}$	
6 300-10/1		 NAND function, i.e. AND function with negated output The output will stand at its 0-state if, and only if, all inputs stand at their defined 1-states. $S = \overline{X\,Y\,Z}$	

1) This form is not preferred for future use (see 5.1).

6.3 Derived combinative functions — Examples (*concluded*)

Code number	Graphical symbol Form A	Description	Graphical symbol Form B[1]
6 300-15/1		X Y Z S 0 0 0 0 0 0 1 0 0 1 0 0 0 1 1 1 1 0 0 0 1 0 1 0 1 1 0 0 1 1 1 0 AND function with one or more negated input(s) The output will stand at its defined 1-state if, and only if, all non-negated inputs stand at their defined 1-states and all negated inputs stand at their 0-states. $S = \overline{X}\,Y\,Z$	
6 300-20/1		X Y Z S 0 0 0 1 0 0 1 1 0 1 0 1 0 1 1 1 1 0 0 0 1 0 1 1 1 1 0 1 1 1 1 1 OR function with one or more negated input(s) The output will stand at its defined 1-state if, and only if, one or more non-negated input(s) stand at their defined 1-states and/or one or more negated inputs stand at their 0-states. $S = X + Y + Z$	
6 300-25/1		X Y Z S 0 0 0 0 0 0 1 1 0 1 0 1 0 1 1 1 1 0 0 0 1 0 1 0 1 1 0 0 1 1 1 0 OR function with one inhibiting input The output will stand at its defined 1-state if, and only if, one or more non-inhibiting input(s) stand at their defined 1-states and the inhibiting input stands at its 0-state. $S = \overline{X}\,(Y + Z)$	
6 300-30/1		X Y Z S 0 0 0 0 0 0 1 0 0 1 0 0 0 1 1 0 1 0 0 0 1 0 1 1 1 1 0 1 1 1 1 1 OR function with one negated inhibiting input The output will stand at its defined 1-state if, and only if, one or more non-negated inhibiting input(s) stand at their defined 1-states and the negated inhibiting input stands at its 1-state. $S = X\,(Y + Z)$	

1) This form is not preferred for future use (see 5.1).