SLOVENSKI STANDARD
SIST EN 61188-1-2:2001

01-marec-2001

Printed boards and printed board assemblies - Design and use - Part 1-2: Generic requirements - Controlled impedance

Printed boards and printed board assemblies - Design and use -- Part 1-2: Generic requirements - Controlled impedance

Leiterplatten und Flachbaugruppen - Konstruktion und Anwendung -- Teil 1-2: Allgemeine Anforderungen - Definierte Impedanz

Cartes imprimées et cartes imprimées équipées - Conception et utilisation -- Partie 1-2: Prescriptions génériques - Impédance contrôlée

Ta slovenski standard je istoveten z: **EN 61188-1-2:1998**

ICS:

31.180	Tiskana vezja (TIV) in tiskane ploġ e	Printed circuits and boards

SIST EN 61188-1-2:2001 **en**

EUROPEAN STANDARD

NORME EUROPÉENNE

EUROPÄISCHE NORM

EN 61188-1-2

August 1998

ICS 31.180

English version

Printed boards and printed board assemblies - Design and use
Part 1-2: Generic requirements - Controlled impedance
(IEC 61188-1-2:1998)

Cartes imprimées et cartes imprimées équipées - Conception et utilisation
Partie 1-2: Prescriptions génériques
Impédance contrôlée
(CEI 61188-1-2:1998)

Leiterplatten und Flachbaugruppen
Konstruktion und Anwendung
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Definierte Impedanz
(IEC 61188-1-2:1998)

This European Standard was approved by CENELEC on 1998-08-01. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the Central Secretariat or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the Central Secretariat has the same status as the official versions.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Czech Republic, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland and United Kingdom.

CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B - 1050 Brussels

Ref. No. EN 61188-1-2:1998 E

Foreword

The text of document 52/758/FDIS, future edition 1 of IEC 61188-1-2, prepared by IEC TC 52, Printed circuits, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 61188-1-2 on 1998-08-01.

The following dates were fixed:

- latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 1999-05-01
- latest date by which the national standards conflicting with the EN have to be withdrawn (dow) 2001-05-01

Annexes designated "normative" are part of the body of the standard.
Annexes designated "informative" are given for information only.
In this standard, annex ZA is normative and annex A is informative.
Annex ZA has been added by CENELEC.

Endorsement notice

The text of the International Standard IEC 61188-1-2:1998 was approved by CENELEC as a European Standard without any modification.

Annex ZA (normative)

Normative references to international publications with their corresponding European publications

This European Standard incorporates by dated or undated reference, provisions from other publications. These normative references are cited at the appropriate places in the text and the publications are listed hereafter. For dated references, subsequent amendments to or revisions of any of these publications apply to this European Standard only when incorporated in it by amendment or revision. For undated references the latest edition of the publication referred to applies (including amendments).

NOTE: When an international publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

Publication	Year	Title	EN/HD	Year
IEC 61182	series	Printed boards - Electronic data description and transfer	-	-
IEC 61182-1	1994	Part 1: Printed board description in digital form	-	-
IEC 61189-3	1997	Test methods for electrical materials, printed boards and other interconnection structures and assemblies Part 3: Test methods for interconnection structures (printed boards)	EN 61189-3	1997

NORME INTERNATIONALE

INTERNATIONAL STANDARD

CEI
IEC
61188-1-2

Première édition
First edition
1998-04

Cartes imprimées et cartes imprimées équipées – Conception et utilisation –

Partie 1-2: Prescriptions génériques – Impédance contrôlée

Printed boards and printed boards assemblies – Design and use –

Part 1-2: Generic requirements – Controlled impedance

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Commission Electrotechnique Internationale
International Electrotechnical Commission
Международная Электротехническая Комиссия

CODE PRIX
PRICE CODE X

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

PRINTED BOARDS AND PRINTED BOARD ASSEMBLIES – DESIGN AND USE –

Part 1-2: Generic requirements – Controlled impedance

FOREWORD

1) The IEC (International Electrotechnical Commission) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of the IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, the IEC publishes International Standards. Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. The IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.

2) The formal decisions or agreements of the IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested National Committees.

3) The documents produced have the form of recommendations for international use and are published in the form of standards, technical reports or guides and they are accepted by the National Committees in that sense.

4) In order to promote international unification, IEC National Committees undertake to apply IEC International Standards transparently to the maximum extent possible in their national and regional standards. Any divergence between the IEC Standard and the corresponding national or regional standard shall be clearly indicated in the latter.

5) The IEC provides no marking procedure to indicate its approval and cannot be rendered responsible for any equipment declared to be in conformity with one of its standards.

6) Attention is drawn to the possibility that some of the elements of this International Standard may be the subject of patent rights. The IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 61188-1-2 has been prepared by IEC technical committee 52: Printed circuits.

The text of this standard is based on the following documents:

FDIS	Report on voting
52/758/FDIS	52/762/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

Annex A is for information only.

INTRODUCTION

Packaging of electronic equipment has traditionally been an area for mechanical considerations. Packaging design is becoming more complex as today's electronics technologies are available in greater switching speed and higher density per chip. Individual chips have greater numbers of connections in smaller chip package sizes. To take maximum advantage of device density and speed, designers must pay much more attention to problems of electromagnetic wave propagation phenomena associated with transmission of switching signals within the system. New design disciplines and design strategies are needed. Controlled impedance printed boards are a part of this strategy.

Interconnection and the packaging of electronic components primarily have been the domain of mechanical designers who were concerned with such factors as weight, volume, power, and form factor and with interconnections specified in wire listing or net lists. Electrical conductors for signal transmission were routed with only a few concerns, that continuity was maintained between points, conductors had sufficient copper for the current and clearance was maintained to prevent voltage breakdown. Aside from providing a good electrical path, the electrical performance of the signal was not a major concern.

Advances in digital integrated circuits introduce new devices with extremely fast rise times which are housed in high density microelectronic packages. In order to optimize system performance, these devices require a wiring technology that supports high density interconnection and, at the same time, provides superior electrical performance.

While many system problems are associated with high speed digital processing, none has received more attention than interconnection. It is evident that as system speeds increase, interconnection, packaging, and printed boards become the bottlenecks that slow system performance. Systems using 100 K ECL circuitry have almost 55 % of the system delay in the packaging and interconnect. CMOS is normally considered a "slow" technology, but is designed into system clock rates in excess of 100 MHz. In these cases, not only is system delay a problem but signal attenuation becomes an issue with the low powered, low voltage, lower noise margin BiCMOS devices.

Chips can be individually mounted on a large board or assembled into small boards or multichip modules mounted onto large boards. Large systems may require several large board assemblies with another level of interconnection. Noise, timing, and signal degradation will accompany transitions from one packaging level to the next.

The electrical connections to the board can be of a variety of configurations ranging from pins that will insert through plated holes in the board, as in dual in-line packages, to a series of lands for surface mount devices. Requirements for component packaging are dependent on many factors including space, economics, electrical performance and reliability, as well as the predominant packaging style of the assembly. The components shall be provided in a style that is compatible with the assembly processes used to manufacture the printed board assembly.

The component package shall be considered when designing for high speed. In passive components the predominant factor will be the lead length as leads provide additional inductance and capacitance that will affect propagation speed and switching transients. To minimize these effects the leads may be as short as possible or removed. Surface mount devices can provide leadless packages which can be directly mounted to the interconnecting substrate.

NOTE – Component data sheets often do not provide parasitic values for high speed noise and propagation speed consideration.

Active devices, components such as integrated circuits, are often offered in several packages. In general, DIP packages, in either plastic or ceramic, have been the predominate package . These are typically the largest packages and provide the poorest high speed operating environment due to lead configuration. The next best package style is the surface mount package. These are offered in a variety of packages such as SOICs, PLCCs, PFQPs, TSOPs BGAs. These packages will typically reduce the lead capacitance and inductance.

To obtain the optimum performance from the device, the die can be directly mounted to the substrate using either the chip-on-board (COB), flip chip or tape automated bonding (TAB) approach. These offer an optimum approach since they minimize the lead capacitance/ inductance.

3.2 Intraconnection

3.2.1 Connectors

Intraconnections are often troublesome in high speed application because a continuous signal environment is not provided. Most board to board connector systems are not designed for use in high performance applications and compromise the signal integrity of the system. Board to board connections often mismatch the characteristic impedance designed into the board themselves.

There are two primary approaches to reduce the signal discontinuity caused by interconnect systems:

a) The first approach is to provide a connector style such that the pinouts can be arranged to provide a good signal path. Non-differential signals shall establish a relationship between the active signal line and the closest reference plane connection, either a voltage or ground plane. Non-differential signal conductors rely on controlled geometries and nearby reference plane for impedance control. Signal pin quality, reference pin quality and their location controls electrical performance. To optimise performance, reference pins shall be added to reduce the cross-talk problems. Generally a 3:1 ratio of signal to reference pins (i.e. 3 signal, 1 reference) is sufficient;

b) The second approach is to modify the connector to minimize the discontinuity. By shortening the pin length, or adding a reference ground plane within the connector, smaller distances between boards can be used.

Board mounted coaxial connectors are frequently used when only a few signal lines are connecting to a circuit board or where either signal isolation or signal integrity is important.

3.2.2 Cables

Discrete coax connectors and cables are often used because they can couple high speed, high frequency signals to a printed board with little signal degradation. There are four areas that shall be considered:

- signal propagation speed;
- cross-talk;
- induced noise;
- impedance matching.

Discrete coaxial wires have been used with discrete wiring boards for unique, high-speed applications up to 18 GHz. An optical cable has also been used successfully with discrete wiring boards for high frequency signals.

3.3 Printed board and printed board assemblies

Component placement is a critical factor in the design of high-speed systems. The effects of unsuitable placement can be significant and include concerns in the following areas:

- cross-talk management;
- impedance control;
- power distribution.

3.3.1 Board design

The number of signal layers in multilayer boards will be influenced by the density of interconnections within the board as well as the effect of cross-talk or coupling between signal lines. Cross-talk allowance can make it necessary to add layers or can require increasing space between conductors decreasing the interconnect density.

Discrete wiring board density of interconnections within the board will influence the effect of cross-talk. The use of diagonal wire routing on the same wiring layers that route conductors vertically or horizontally (i.e. X and Y directions) may allow greater circuit density per layer and the placement geometries available can accommodate high density and low cross-talk.

A close relationship between design and performance exists in the case of interconnection lines involving high speed digital signals. This interdependence did not exist previously or could be ignored in low-speed signal applications, however, it now imposes new design rules, restrictions and process controls.

To meet the challenges of high-speed digital processing, today's multilayer printed board shall:

- reduce propagation delay;
- lower cross-talk and other line parasitics;
- reduce signal loss;
- allow for high density interconnections.

To achieve these desired goals the designer shall start by controlling the impedance of the transmission lines.

Controlled conductors on boards can be used for signal interconnect between devices. For a given construction, impedance can be controlled with a specific dielectric thickness, conductor thickness, conductor width and the relative permittivity (dielectric constant).

Board substrate selection, relative permittivity (dielectric constant) (ε_r) effects signal propagation and thickness for a given characteristic impedance as well as line width. Lower ε_r results in faster signal propagation, but increases conductor width for a given impedance value.

For discrete wired boards the conductor thickness and width is controlled by selection of the appropriate wire size. The insulation on the discrete wires can result in a lower effective relative permittivity (dielectric constant) for a given construction, resulting in higher signal propagation speeds in discrete wire boards. Designing to specific impedance values, controls (as transmission lines) the capacitance and the material between conductors. Signal paths should be kept short to minimize propagation delays. Even if it were possible to make a circuit capable of switching at infinite speed, the interconnection material would dictate the performance of the systems. Figure 1 illustrates the switching speed of a device versus propagation delay in a typical woven glass epoxide dielectric commonly used in the printed board industry.

Space constraints, number and complexity of interconnections, power distribution and cost of manufacture are some factors to be considered. When determining requirements of layer count the thickness of dielectric layers, the composition and thickness of ground/voltage plane layers, the dielectric composition, conductor width/thickness and the overall length. The width and thickness of the conductor will determine manufacturing costs.

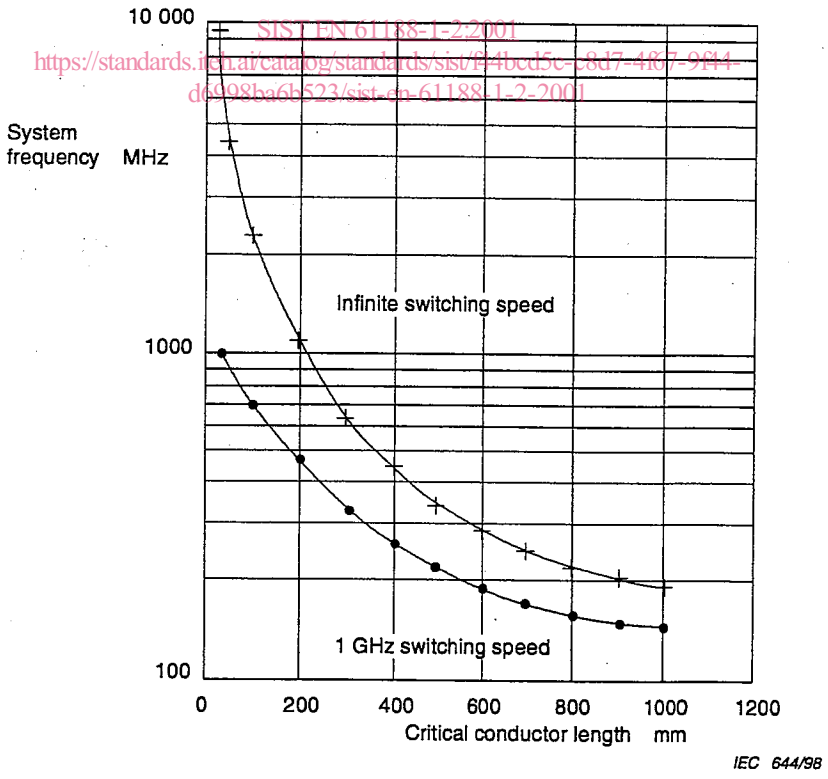

Figure 1 – Switching speed versus propagation delay