INTERNATIONAL STANDARD

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First edition
2006-08

**Semiconductor devices –
Integrated circuits –**

**Part 4-3:
Interface integrated circuits – Dynamic criteria for analogue-digital converters (ADC)**

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SEMICONDUCTOR DEVICES –
INTEGRATED CIRCUITS –

Part 4-3: Interface integrated circuits –
Dynamic criteria for analogue-digital converters (ADC)

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International Standard IEC 60748-4-3 has been prepared by subcommittee 47A: Integrated circuits, of IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the following documents:

FDIS	Report on voting
47A/750/FDIS	47A/758/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

The list of all the parts of the IEC 60748 series, under the general title *Semiconductor devices – Integrated circuits*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

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INTRODUCTION

The use of ADCs has increased significantly in the last few years with the large increase in the use of digital signal processing. The majority of the processing of analogue signals now takes place in the digital domain, and this requires high precision in the conversion of signals from the analogue to the digital form. Consequently, the characterization of ADCs is of great importance.

IEC 60748-4 contains measuring methods for ADCs in which the test conditions are either static or change very slowly. However, some of the characteristics of an ADC can change to some degree with the rate of change of the input signal, and there are other characteristics that cannot be measured except under dynamic conditions. Consequently, a set of dynamic tests is required in order to obtain the response of an ADC when operated under dynamic conditions.

The output of a dynamic test consists of the set of output code values obtained during the test. This record, being the sequence in time of a set of values, gives information in the “time-domain”. The result of applying the Fourier Transform to the record is information that is in the “frequency domain”, and this contains the spectrum of the output over the range of frequencies of interest. In particular, distortion, noise and spurious output frequencies can then be evaluated.

This International Standard introduces a set of dynamic methods, which are now coming into use in industry and which rely mostly on measurements made with sinusoidal input signals, and of which the results are suitable for analysis in the frequency domain. It also includes a further dynamic method that uses a wide-band input signal. For the reasons explained below, industry has shown great interest in this particular method.

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Linearity errors of an ADC are dependent on the amplitude of the input signal and its rate of change. Not so well known is that linearity errors also depend on the instantaneous amplitude distribution, i.e. amplitude probability density function (APDF) of the input signal. This source of error is usually a result of localized heating effects in the integrated circuit and is dependent on ADC architecture and internal circuit layout.

Single-frequency signals have an APDF concentrated at the extremes and therefore exaggerate the effect of errors at the ends of the input range compared to those nearer the centre. Conversely, a wide-band signal has an APDF concentrated more around the centre of the input range. A wide-band signal is much closer to the typical input signal in the majority of ADC applications than a single-frequency signal. Therefore, measurements made with such a signal will give more realistic error estimates.

A wide-band signal can be generated from a pseudo-random binary sequence. Although such a signal appears to be noisy, it contains only a set of defined frequencies and is therefore suitable for measuring errors.

SEMICONDUCTOR DEVICES –
INTEGRATED CIRCUITS –

Part 4-3: Interface integrated circuits –
Dynamic criteria for analogue-digital converters (ADC)

1 Scope

This part of IEC 60748 specifies a set of measuring methods and requirements for testing ADCs under dynamic conditions, together with associated terminology and characteristics.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60748-4:1997, *Semiconductor devices – Integrated circuits – Part 4: Interface integrated circuits*

IEC 60268-10:1991, *Sound system equipment – Part 10: Peak programme level meters*

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3 Terms and definitions

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For the purposes of this document, the following definitions, in addition to those found in Chapter II, Clause 2, Terms for category II of IEC 60748-4:1997, apply.

3.1
coherent sampling
process in which the output record contains samples taken from an integral number of input cycles of a repetitive waveform

NOTE In general, this process is limited to the case where the number of input cycles and the number of samples in the record have no common factors.

3.2
equivalent-time sampling
coherent sampling in which consecutive samples of a repetitive waveform, acquired from multiple repetitions of the waveform, are assembled and re-arranged to produce a single record of samples that represent a single repetition of the waveform

NOTE This process is normally used only when the spectrum of the input waveform contains significant amounts of energy at frequencies above half the sampling frequency. It has the result that each frequency in the input appears in the output divided by the number of repetitions. For each successive input cycle, the set of samples is delayed (or advanced) relative to the previous set by a fixed amount.

3.3
(code) transition value
boundary between two adjacent steps

3.4
signal-to-noise-and-distortion ratio
for a pure sine-wave input, ratio of the r.m.s. amplitude of the output signal at the input frequency to the r.m.s. amplitude of all other signals in the output

3.5

(spurious-free) dynamic range

for a pure sine-wave input, ratio of the r.m.s. amplitude of the output signal at the input frequency to the largest r.m.s. amplitude of the output at any other single frequency

3.6

effective number of bits

N_{ef}

practical limit of the resolution of an ADC due to inherent noise and errors

3.7

signal-dependent timing error

effect equivalent to the delay of the instant of sampling, in an ADC, that is proportional to the rate of change of input voltage

NOTE This effect is caused by the inherent voltage-dependent non-linearity of circuit elements in semiconductors.

3.8

spurious frequency

persistent sine wave in the output that is not considered to be a harmonic of the input frequency

3.9

word error rate

probability of an output code having an error not attributable to random noise or to offset, gain, and linearity errors

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4 Characteristics

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The following characteristics shall be included as characteristics applicable to ADCs and should be read with reference to Chapter III, Section 2, Category II, Clause 4 of IEC 60748-4:1997.

Ref.	Characteristic	Conditions at 25 °C unless specified otherwise	Letter Symbol	Notes	Requirements	
					Max.	Min.
4.1	Settling time	Supply voltages Input step amplitude Specified levels for transition time Clock frequency, as appropriate Conditions at other terminals Tolerance for settling time	t_{tot}		X	
4.2	Long-term settling error		E_{LT}		X	
4.3	Rise and fall times		t_r; t_f		X	
4.4	Limiting rate of change of output (slew rate)		$(\Delta v/\Delta t)_{max}$, SR			X
4.5	Overload recovery times					
4.5.1	Input overload recovery time, where appropriate	Supply voltages Input signal frequency, as appropriate Input signal amplitude Overload signal amplitude and duration Clock frequency, as appropriate Conditions at other terminals	t_{or}		X	
4.5.2	Differential-mode input overload recovery time, where appropriate		t_{ord}		X	
4.5.3	Common-mode input overload recovery time, where appropriate		t_{orc}		X	
4.6	Differential gain, where appropriate	Supply voltages Input signal frequency, as appropriate Input signal amplitude Clock frequency, as appropriate DC input levels Conditions at other terminals Desired accuracy	A_{dif}		X	
4.7	Differential phase, where appropriate		ϕ_{dif}		X	
4.8	Total harmonic distortion	Supply voltages Input signal frequency, as appropriate Input signal amplitude Clock frequency, as appropriate Highest harmonic excluded from noise, if not 10th Conditions at other terminals	THD		X	
4.9	Spurious-free dynamic range		SFDR			X
4.10	Signal-to-noise-and-distortion ratio		SINAD			X
4.11	Effective number of bits		N_{ef}			X
4.12	Signal-to-noise ratio		SNR			X
4.13	Noise floor		NF		X	
4.14	Signal-dependent timing error		E_{SDT}		X	

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5 Measuring methods

5.1 Dynamic testing with sinusoidal signals

The following methods are to be read with reference to Chapter IV, Section 3, Category II, Group I of IEC 60748-4:1997. All references below to IEC 60748-4:1997 apply to this clause.

5.1.1 Dynamic testing of ADCs – General requirements

5.1.1.1 Purpose

To specify the general requirements for measuring the characteristics of an ADC under dynamic conditions.

5.1.1.2 Circuit diagram

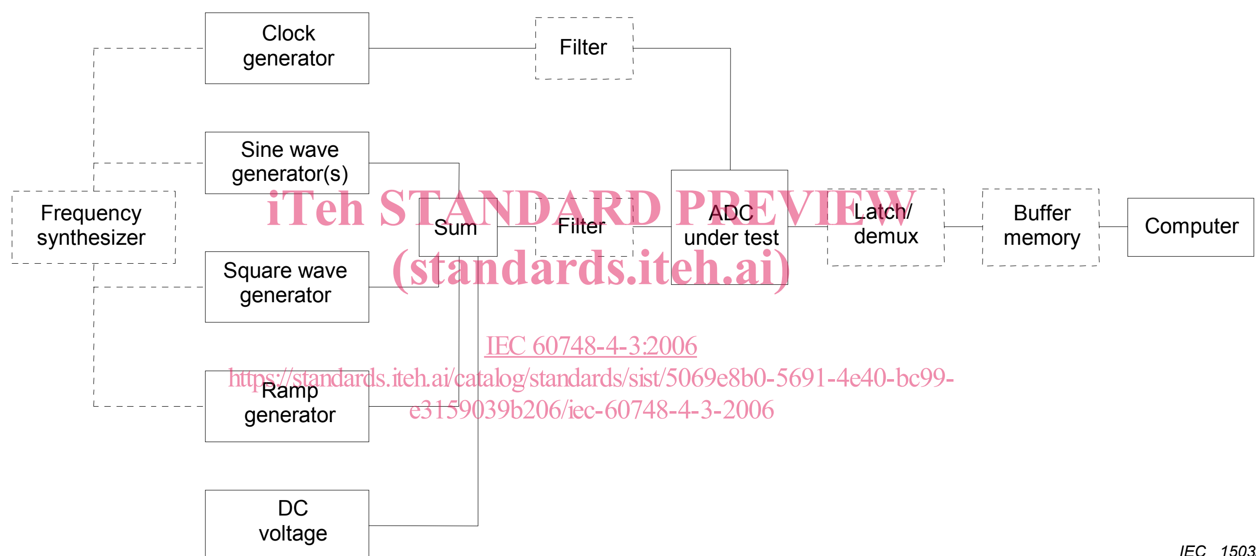

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Figure 1 – Test arrangement for measurements on ADCs under dynamic conditions

Optional elements are shown in broken outline.

5.1.1.3 Circuit description and requirements

– Case a) sine wave input

The input voltage generator shall provide an accurate sinusoidal waveform with adjustable and stable amplitude and frequency.

– Case b) step input

The input voltage generator shall provide a stepped wave, usually a square wave, without droop, and with adjustable and stable levels, duty-cycle and periodicity.

– Case c) linear input ramp

The input voltage generator shall provide an accurate linear rising and/or falling waveform with adjustable and stable amplitude, duty-cycle and periodicity.

– All cases:

Precautions shall be taken to avoid coupling between the sampling clock and the input circuits, and between the output and input circuits, and the networks used to combine input signals shall be designed to minimize any stray reactive elements that could affect the bandwidth of applied signals.

Noise at the input should be small compared with the output noise that is generated within the ADC, and preferably no larger in magnitude than the noise that results from the quantization process, i.e. significantly less than 1 LSB in magnitude. When necessary, and normally only for sine waves, input noise can be reduced by passing the signal through a low-pass or band-pass filter. The latter may also be used to reduce any frequency instability in the signal.

Any impurity in the signal waveform and instability in its frequency should be low enough not to affect the accuracy of the measurements. Similarly, any instability in the frequency (jitter) of the clock signal should be equally low. Ideally, the input signal and the clock signal should be synchronized from a common source.

The adjustment range of the input voltage should be such that, at its maximum excursion, the most positive and most negative peaks exceed the working range of the ADC, but do not exceed its limiting input voltages.

Equipment shall be included for the adjustment of offset and gain points of adjustable converters.

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For some measurements, both step and sinusoidal inputs are applied together to the ADC.

The recording equipment should be capable of storing each output code obtained during the test duration. In cases where this is physically not possible, or accuracy is reduced in a long test duration due to frequency instability, then the test may be divided into a set of segments of equal length, where the record of each segment is analysed separately, provided that for each segment the phase of the input signal at its start is either randomly chosen or uniformly distributed within the range 0..2π.

For analysis of the histogram of the ADC output, the recording equipment shall count the number of occurrences of each individual output code value during the test. The test duration should be such that each output code value appears enough times to achieve the required accuracy (see Figures 3 and 4 and also Annex A) to determine a suitable number.

For analysis of the spectrum of the ADC output, the recording equipment shall record the code value of each individual sample during the test.

5.1.1.4 Special precautions regarding accuracy

Note the comments above regarding signal purity, frequency stability, and input noise.

In order that each test is carried out with coherent sampling, the duration of each segment of the test shall be set to an integral number of input cycles. However, the periodicity or frequency of the input waveform and that of the sampling clock shall not have a common factor, thus

$$f_i = f_s \cdot J/M \quad (1)$$

where

f_i is the input frequency;

f_s is the sampling frequency;

M is the number of samples in a test record;

J is the number of input periods in a test record, an integer,

the fraction J/M shall be irreducible.

If the requirement for J to be an integer is not met, then the method of analysis will give large errors. Although there is a mathematical procedure that can extract reasonably accurate results when J is not an integer, its use is outside the scope of this standard.

In general, J will be an odd number greater than 1, and M an even number. For certain cases, detailed below (see 5.1.1.5), M should be a power of 2.

Ideally for analysis of the spectrum, each output code should appear at least once in the output record. There are $2N$ possible output codes, when N is the number of bits. In the case of sine-wave input (and a linear ADC), for each output code to appear at least once, it is required that

$$M \geq \pi \cdot 2N \tag{2}$$

When it is required that the input frequency should be very close to a particular input frequency (f_i), then proceed as follows: find an integer, r, near to f_s/f_i, let J equal the integral part of M/r, then

$$fi = fs \cdot J/(r \cdot J - 1) \tag{3}$$

and

$$= r \cdot J - 1 \tag{4}$$

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5.1.1.4.1 Histogram testing

For tests that determine the transfer characteristic, and thereby the linearity errors, the dynamic method involves obtaining a histogram of output codes. Provided that the input signal is sufficiently free from error, accuracy increases with the number of samples recorded for each code value. Specific requirements to achieve the required accuracy are given in the corresponding method.

5.1.1.4.2 Spectral analysis

For spectral analysis, provided that M is sufficient to give at least one sample for each code value, the accuracy increases with $\sqrt{M}$, but the error due to frequency instability increases with the product of both J and M, thus J should not be large. Where an increase in accuracy is desired, then multiple records, starting at different points in the input waveform, may be used to give an improvement proportional to $\sqrt{R}$, where R is the number of records. In this case, it is usual to compute the required terms separately for each record and take the average over all the records of each term.

To take account of variations in actual step width, frequency instability and jitter, the value of M should be increased from the theoretical minimum, so that

$$M \geq \frac{\pi \cdot 2^N}{\left(1 - K \cdot \sigma_\phi\right) \cdot \left(1 - \left|E_{Dmax}\right|\right)} \tag{5}$$

where

N is the number of bits of the ADC;

K is the number of standard deviations that give the required confidence level (see Table 1);

σ_ϕ is the r.m.s. value of combined phase jitter, referred to the clock period;

E_{Dmax} is the maximum value of differential linearity error.