



SLOVENSKI STANDARD
SIST EN 61964:2002
01-september-2002

Integrated circuits - Memory devices pin configurations

Integrated circuits - Memory devices pin configurations

Integrierte Schaltungen - Kontaktanordnungen für Speicherbauelemente

Circuits intégrés - Configuration de broches de mémoires

Ta slovenski standard je istoveten z: EN 61964:1999

[SIST EN 61964:2002](https://standards.iteh.ai/catalog/standards/sist/4bc05e4c-572a-4b19-9ce1-ab75a8d289f8/sist-en-61964-2002)

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ICS:

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EUROPEAN STANDARD
NORME EUROPÉENNE
EUROPÄISCHE NORM

EN 61964

May 1999

ICS 31.200

English version

**Integrated circuits - Memory devices pin configurations
(IEC 61964:1999)**

Circuits intégrés - Configuration
de broches de mémoires
(CEI 61964:1999)

Integrierte Schaltungen
Kontaktanordnungen für
Speicherbauelemente
(IEC 61964:1999)

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This European Standard was approved by CENELEC on 1999-05-01. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the Central Secretariat or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the Central Secretariat has the same status as the official versions.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Czech Republic, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland and United Kingdom.

CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B - 1050 Brussels

Foreword

The text of document 47A/535/FDIS, future edition 1 of IEC 61964, prepared by SC 47A, Integrated circuits, of IEC TC 47, Semiconductor devices, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 61964 on 1999-05-01.

The following dates were fixed:

- latest date by which the EN has to be implemented
at national level by publication of an identical
national standard or by endorsement (dop) 2000-02-01
- latest date by which the national standards conflicting
with the EN have to be withdrawn (dow) 2002-05-01

Annexes designated "normative" are part of the body of the standard.
Annexes designated "informative" are given for information only.
In this standard, annex ZA is normative and annex A is informative.
Annex ZA has been added by CENELEC.

Endorsement notice

The text of the International Standard IEC 61964:1999 was approved by CENELEC as a European Standard without any modification.

In the official version, for annex A, Bibliography, the following note has to be added for the standard indicated:

IEC 60749 <https://standards.iteh.ai/catalog/standards/sist/4bc05e4c-572a-4b19-9ce1-ab75ab82874b/sist-en-61964-2002>
NOTE: Harmonized as EN 60749:1999 (not modified).

Annex ZA (normative)**Normative references to international publications
with their corresponding European publications**

This European Standard incorporates by dated or undated reference, provisions from other publications. These normative references are cited at the appropriate places in the text and the publications are listed hereafter. For dated references, subsequent amendments to or revisions of any of these publications apply to this European Standard only when incorporated in it by amendment or revision. For undated references the latest edition of the publication referred to applies (including amendments).

NOTE: When an international publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

<u>Publication</u>	<u>Year</u>	<u>Title</u>	<u>EN/HD</u>	<u>Year</u>
IEC 60191-2	1966	Mechanical standardization of semiconductor devices Part 2: Dimensions	-	-
IEC 60748-1	1984	Semiconductors devices - Integrated circuits Part 1: General	-	-

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INTERNATIONALE
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CEI
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Première édition
First edition

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Configuration de broches de mémoires**

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Commission Electrotechnique Internationale
International Electrotechnical Commission
Международная Электротехническая Комиссия

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

**INTEGRATED CIRCUITS –
MEMORY DEVICES PIN CONFIGURATIONS**
FOREWORD

- 1) The IEC (International Electrotechnical Commission) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of the IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, the IEC publishes International Standards. Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. The IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
- 2) The formal decisions or agreements of the IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested National Committees.
- 3) The documents produced have the form of recommendations for international use and are published in the form of standards, technical reports or guides and they are accepted by the National Committees in that sense.
- 4) In order to promote international unification, IEC National Committees undertake to apply IEC International Standards transparently to the maximum extent possible in their national and regional standards. Any divergence between the IEC Standard and the corresponding national or regional standard shall be clearly indicated in the latter.
- 5) The IEC provides no marking procedure to indicate its approval and cannot be rendered responsible for any equipment declared to be in conformity with one of its standards.
- 6) Attention is drawn to the possibility that some of the elements of this International Standard may be the subject of patent rights. The IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 61964 has been prepared by subcommittee 47A: Integrated circuits, of IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the following documents:

FDIS	Report on voting
47A/535/FDIS	47A/549/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

Annex A is for information only.

INTRODUCTION

The registration and standardization of the mechanical outlines for integrated memory circuit devices is an ongoing activity covered in the IEC 60191 series.

Due to the fact that the same mechanical package can house different types of memory devices, and because the same memory device can be incorporated into different types of mechanical packages, the number of such configurations has to be limited to minimum required by the electronics industry. Registration and standardization of such electrical pinout configurations also helps to establish and maintain compatibility of devices from different vendors and in different applications.

Owing to the nature of the integrated memory circuits business, in which there is ongoing potential for the development of new density generations and new electrical functions, this International Standard has to take the form of an open Standard. In the present context, this signifies that the new items can be added at any time to any of its clauses. New subclauses may be created as new types of memory devices come into usage in the industry.

Additions, deletions and any changes will be subject to agreement in order to become effective for publication.

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INTEGRATED CIRCUITS – MEMORY DEVICES PIN CONFIGURATIONS

1 Scope

This International Standard applies to pinout package configurations of solid state integrated circuit memory devices. The purpose of this standard is to establish a registration procedure for such configurations.

2 Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this International Standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this International Standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies. Members of IEC and ISO maintain registers of currently valid International Standards.

IEC 60191-2:1996, *Mechanical standardization of semiconductor devices – Part 2: Dimensions*

IEC 60748-1:1984, *Semiconductor devices – Integrated circuits – Part 1: General*

<https://standards.iteh.ai/catalog/standards/sist/4bc05e4c-572a-4b19-9ce1-ab75a8d289f8/sist-en-61964-2002>

3 Terms and definitions

For the purpose of this International Standard, the following terms and definitions apply. This contains definitions of a number of terms that are needed for a clear understanding of the standard.

Most of these terms have been developed within the semiconductor memory industry. They are given for quick reference and are not intended to supersede any existing definitions in previous IEC publications such as IEC 60748-1.

The following pin names and functional descriptions apply uniformly to all devices covered by this standard. Where a pin has a dual function, and those functions are invoked at substantially different times, the names and symbols for these functions are separated by a slash (/) (e.g. $V_{PP}/G\backslash$). Where a pin has multiple functions which are used simultaneously, the slash is omitted (e.g. DQ). Where multiple pins have a similar function, a number symbolised as (n) is appended to the symbol. Where the pin function has an inverted logic sense, that is, the function is true or invoked for a low signal, the reverse slash (\) is appended to the symbol. Where alternative functions are permitted by this standard, these authorized functions are listed and separated by commas. Where common usage has resulted in two terms being used interchangeably, both are listed but the less favoured term is enclosed in parentheses.