SLOVENSKI STANDARD
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Family specification: AC MOS Digital integrated circuits

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Familienspezifikation: AC MOS digitale integrierte Schaltungen

Spécification de famille: Circuits intégrés logiques AC MOS

Ta slovenski standard je istoveten z: **EN 190116:1993**

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Familienspezifikation

This European Standard was approved by CENELEC Electronic Components Committee (CECC) on 06 December 1992. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

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This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the CECC General Secretariat has the same status as the official versions.

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CECC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B-1050 Brussels

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Foreword

The CENELEC Electronic Components Committee (CECC) is composed of those member countries of the European Committee for Electrotechnical Standardization (CENELEC) who wish to take part in a harmonized System for electronic components of assessed quality.

The object of the System is to facilitate international trade by the harmonization of the specifications and quality assessment procedures for electronic components, and by the grant of an internationally recognized Mark, or Certificate, of Conformity. The components produced under the System are thereby acceptable in all member countries without further testing.

This European Standard was prepared by CECC WG 9, "Integrated circuits".

The text of the draft based on document CECC (Secretariat) 3120 was submitted to the formal vote; together with the voting report, circulated as document CECC (Secretariat) 3275 it was approved by CECC as EN 190116 on 06 December 1992.

The following dates were fixed:

- latest date of announcement of the EN at national level (doa) 1994-01-11
- latest date of publication of an identical national standard (dop) 1994-07-11
- latest date of declaration of national standards obsolescence 1994-07-11
- latest date of withdrawal of conflicting national standards (dow) 2004-01-11

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ELECTRONIC COMPONENTS OF ASSESSED QUALITY IN ACCORDANCE WITH : CECC 90 000 : Generic specification for monolithic integrated circuits (GS). CECC 90 100 : Sectional specification for digital monolithic integrated circuits (SS).	
OUTLINE AND DIMENSIONS (See DS for the specific type) TERMINAL CONNECTIONS (See DS for the specific type)	**FAMILY SPECIFICATION FOR AC MOS DIGITAL INTEGRATED CIRCUITS** **54/74 AC** **54/74 ACT** TYPICAL CONSTRUCTION : Silicon complementary MOS, isoplanar silicon gate types with C MOS compatible inputs (AC types) or TTL compatible inputs (ACT types), cavity packages. CAUTION : These are electrostatic sensitive devices. ASSESSMENT LEVELS : P, Y

CONTENTS

1 LIMITING CONDITIONS OF USE FOR THE FAMILY

2 RECOMMENDED OPERATING CONDITIONS AND ASSOCIATED CHARACTERISTICS FOR THE FAMILY

3 TEST METHODS AND PROCEDURES - MECHANICAL DATA

4 INSPECTION REQUIREMENTS

Information about manufacturers who have components qualified to detail specification written in accordance with this family specification is available in the current CECC 00 200 : Qualified Products List.

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1 Limiting conditions of use for the family (Not for inspection purposes)

1.1 Maximum supply voltage positive

V_{DD} = + 6 V

1.2 Maximum supply voltage negative

V_{CC} = – 0,5 V

1.3.1 ***Maximum dc input protection diode current***

I_{IK} = ± 20 m A

OR (whichever is the worst case)

1.3.2 ***Maximum input voltage***

$V_I = V_{DD}$ + 0,5 V[1)]

1.4.1 ***Maximum dc output diode current***

I_{OK} = ± 50 mA

OR (whichever is the worst case)

1.4.2 ***Maximum output voltage***

$V_O = V_{DD}$ + 0,5 V[1)]

1.5 Maximum dc output source or sink current per output pin

I_O = ± 50 mA

1.6 Maximum dc, supply I_{DD} or I_{SS} pin current

I_{DD} or I_{GND} = ± 100 mA

(For up to four outputs per device add ± 25 mA for each additional output).

1.7 Ambient operating temperature range T_{amb}

74 AC/ACT: 0 °C to + 70 °C

54 AC/ACT: – 55 °C to + 125 °C

1.8 Storage temperature range T_{stg}

– 65 °C to + 150 °C

2 Recommended operating and associated characteristics for the family

(Not for inspection purposes)

These conditions apply over the operating temperature range, unless otherwise specified in the DS.

All voltages are referenced to ground.

AC SERIES: Operating supply voltages V_{DDB} = 3 V(*) to V_{DDA} = 5,5 V

* *No parametric or switching characteristics are specified at V_{DD} less than 3 V.*

At V_{DD} between 2 V and 3 V the output conditions will stay at their previous state so battery back-up is allowed for data retention at these voltages, with the following conditions:

$V_{IH} \geq 0{,}7\ V_{DD}$; $V_{IL} \leq 0{,}3\ V_{DD}$; $V_{OH} \geq 0{,}7\ V_{DD}$ (I_{OH} = – 20 μA) and

$V_{OL} \leq 0{,}3\ V_{DD}$($I_{OL}$ = + 20 μA)

1) Unless otherwise specified in the detail specification.

Table 1 — AC series

Parameters	Symbol	V_{DD} (V)	54/74 AC						Unit
			T_{amb} min.		+ 25 °C		T_{amb} max.		
			min.	max.	min.	max.	min.	max.	
CONDITIONS OF TEST									
2.1 High level input voltage	V_{IHB}	3,0	2,1		2,1		2,1		V
		4,5	3,15		3,15		3,15		V
		5,5	3,85		3,85		3,85		V
2.2 Low level input voltage	V_{ILA}	3,0		0,9		0,9		0,9	V
		4,5		1,35		1,35		1,35	V
		5,5		1,65		1,65		1,65	V
DC PARAMETERS TO BE VERIFIED IN SUB-GROUP A3, A4a, A4b									
2.3 Quiescent supply current $V_I = 0$ V or V_{DD} $I_O = 0$ μA	I_{DDA} [a]	5,5		8,0		8,0		80,0	μA
2.4 High level output voltage $V_I = V_{IHB}$ or V_{ILA}	V_{OHB} [b]								
2.4.1 $I_O = -50$ μA		3,0	2,9		2,9		2,9		V
		4,5	4,4		4,4		4,4		V
		5,5	5,4		5,4		5,4		V
2.4.2 $I_O = -12$ mA		3,0	2,4		2,56		2,4		V
2.4.3 $I_O = -24$ mA		4,5	3,7		3,86		3,7		V
		5,5	4,7		4,86		4,7		V
2.5 Low level output voltage $V_I = V_{IHB}$ or V_{ILA}	V_{OLA} [b]								
2.5.1 $I_O = +50$ μA		3,0		0,1		0,1		0,1	V
		4,5		0,1		0,1		0,1	V
		5,5		0,1		0,1		0,1	V
2.5.2 $I_O = +12$ mA		3,0		0,4		0,36		0,50	V
2.5.3 $I_O = +24$ mA		4,5		0,4		0,36		0,50	V
		5,5		0,4		0,36		0,50	V
2.6 Positive a) and negative b) input clamping voltage a) GND open, $V_{DD} = 0$ V b) V_{DD} open, GND = 0 V $\lvert I_{IK} \rvert = 1$ mA	$\lvert V_{IK} \rvert$					0,4	1,5		V
2.7 Input leakage current $V_I = 0$ V or V_{DD}	$\lvert I_{I(off)A} \rvert$	5,5		0,1		0,1		1,0	μA

[a] Unless otherwise specified in the DS
[b] Not applicable to open drain outputs

Table 1 — AC series

Parameters	Symbol	V_{DD} (V)	54/74 AC						Unit
			T_{amb} min.		+ 25 °C		T_{amb} max.		
			min.	max.	min.	max.	min.	max.	
2.8 3-state output off-state current $V_I = V_{DD}$ or 0 V $V_O = 0$ V for I_{OZL} $V_O = V_{DD}$ for I_{OZH}	$\lvert I_{OZA} \rvert$	5,5		0,5		0,5		10,0	μA
CAPACITANCE TO BE VERIFIED IN SUB-GROUP D5									
2.9 Power dissipation capacitance	C_{PDA} [a]	5,5			[a]				pF
ADDITIONAL INFORMATION (Not for inspection purpose)									
2.10 Noise margin at low level output $(V_{ILA} - V_{OLA})$ $I_O = +50\ \mu$A	V_{NLB}	3,0 4,5 5,5	0,8 1,25 1,55		0,8 1,25 1,55		0,8 1,25 1,55		V V V
2.11 Noise margin at high level output $(V_{OHB} - V_{IHB})$ $I_O = -50\ \mu$A	V_{NHB}	3,0 4,5 5,5	0,8 1,25 1,55		0,8 1,25 1,55		0,8 1,25 1,55		V V V
2.12 Input rise and fall time between V_{ILA} and V_{IHB}	t_r, t_f [b]	3,6 to 5,5		8,0		8,0		8,0	ns/V
2.13 Maximum continuous internal power dissipation with reference to derating curve or factor related to reference point temperature or ambient temperature	P_{DA} Reduction factor (mW/°C)	$T_{jA} = 150$ °C Case DG: $P_{DA} = 1,25$ W f = 10 mW/°C Case PC: $P_{DA} = 1,25$ W f = 11 mW/°C							

[a] See measurement method in clause 3.4 here after and limits for each type in the relevant DS.
[b] Except for Schmitt inputs.

Table 2 — ACT series

Operating supply voltages V_{DDB} = 4,5 V to V_{DDA} = 5,5 V

Parameters	Symbol	V_{DD} (V)	54/74 ACT						Unit
			T_{amb} min.		+ 25 °C		T_{amb} max.		
			min.	max.	min.	max.	min.	max.	
CONDITIONS OF TEST									
2.1 High level input voltage	V_{IHB}	4,5 5,5	2,0 2,0		2,0 2,0		2,0 2,0		V V
2.2 Low level input voltage	V_{ILA}	4,5 5,5		0,8 0,8		0,8 0,8		0,8 0,8	V V
DC PARAMETERS TO BE VERIFIED IN SUB-GROUP A3, A4a, A4b									
2.3 Quiescent supply current 2.3.1 V_I = 0 V or V_{DD} I_O = 0 µA	I_{DDA} [a]	5,5		8,0		8,0		80,0	µA
2.3.2 Additional worst case supply current per input I_O = 0 µA One input at: $V_I = V_{DD} - 2,1$ V others at: V_I = 0 V or V_{DD}	ΔI_{DDT}	5,5		1,6		1,6		1,6	mA
2.4 High level output voltage $V_I = V_{IHB}$ or V_{ILA}	V_{OHB} [b]								
2.4.1 I_O = – 50 µA		4,5 5,5	4,4 5,4		4,4 5,4		4,4 5,4		V V
2.4.2 I_O = – 24 mA		4,5 5,5	3,7 4,7		3,86 4,86		3,7 4,7		V V
2.5 Low level output voltage $V_I = V_{IHB}$ or V_{ILA}	V_{OLA} [b]								
2.5.1 I_O = + 50 µA		4,5 5,5		0,1 0,1		0,1 0,1		0,1 0,1	V V
2.5.2 I_O = + 24 mA		4,5 5,5		0,4 0,4		0,36 0,36		0,5 0,5	V V
2.6 Positive a) and negative b) input clamping voltage a) GND open, V_{DD} = 0 V b) V_{DD} open, GND = 0 V $\lvert I_{IK} \rvert$ = 1 mA	$\lvert V_{IK} \rvert$				0,4	1,5			V

[a] Unless otherwise specified in the DS
[b] Not applicable to open drain outputs.

Table 2 — ACT series

Parameters	Symbol	V_{DD} (V)	54/74 ACT						Unit
			T_{amb} min.		+ 25 °C		T_{amb} max.		
			min.	max.	min.	max.	min.	max.	
2.7 Input leakage current V_I = 0 V or V_{DD}	$\lvert I_{I(off)A} \rvert$	5,5		0,1		0,1		1,0	µA
2.8 3-state output off-state current $V_I = V_{DD}$ or 0 V; V_O = 0 V for I_{OZL}; $V_O = V_{DD}$ for I_{OZH}	$\lvert I_{OZA} \rvert$	5,5		0,5		0,5		10,0	µA
CAPACITANCE TO BE VERIFIED IN SUB-GROUP D5									
2.9 Dissipation power capacitance	C_{PDA} [a]	5,5			[a]				pF
ADDITIONAL INFORMATION (not for inspection purpose)									
2.10 Noise margin at low level output ($V_{ILA} - V_{OLA}$) I_O = + 50 µA	V_{NLB}	4,5 5,5	0,7 0,7		0,7 0,7		0,7 0,7		V V
2.11 Noise margin at high level output ($V_{OHB} - V_{IHB}$) I_O = – 50 µA	V_{NHB}	4,5 5,5	2,4 3,4		2,4 3,4		2,4 3,4		V V
2.12 Input rise and fall time between V_{ILA} and V_{IHB}	t_r, t_f [b]	4,5 5,5		10,0 10,0		10,0 10,0		10,0 10,0	ns/V ns/V
2.13 Maximum continuous internal power dissipation with reference to rating curve or factor related to reference point temperature or ambient temperature	P_{DA} Reduction factor (mW/°C)	T_{jA} = + 150 °C Case DG = P_{DA} = 1,25 W f = 10 mW/°C Case PC = P_{DA} = 1,25 W f = 11 mW/°C							

[a] See measurement method in clause 3.4 here after and limits for each type in the relevant DS.
[b] Except for Schmitt inputs.

2.14 Functional test conditions for Sub-Group A2

Input levels 1 or 0 are applied to each test of the functional verification sequence, and the corresponding output levels 1 or 0 are successively verified.

2.14.1 *54/74 AC Series*

$I_{OH} = -1$ mA; $I_{OL} = 1$ mA

$V_{DD} = 3{,}0$ V	Inputs	{1 = 2,5 V {0 = 0,5 V	Outputs	{0 < 0,6 V {1 > 2,4 V
$V_{DD} = 4{,}5$ V	Inputs	{1 = 3,7 V {0 = 0,8 V	Outputs	{0 < 0,9 V {1 > 3,6 V
$V_{DD} = 5{,}5$ V	Inputs	{1 = 4,5 V {0 = 1,0 V	Outputs	{0 < 1,1 V {1 > 4,4 V

2.14.2 *54/74 ACT Series*

$I_{OH} = -1$ mA; $I_{OL} = 1$ mA

$V_{DD} = 4{,}5$ V	Inputs	{1 = 2,4 V {0 = 0,4 V	Outputs	{0 < 0,9 V {1 > 3,6 V
$V_{DD} = 5{,}5$ V	Inputs	{1 = 2,4 V {0 = 0,4 V	Outputs	{0 < 1,1 V {1 > 4,4 V

2.15 Dynamic characteristics (54/74 AC, 54/74 ACT series)

2.15.1 *Pulse generator and driving circuit*

The following conditions shall be met:

— Output impedance of pulse generator: 50 Ω ± 10 %;

— Impedance of the driving circuit cable from the generator, including the test equipment: 50 Ω ± 10 %;

— Low level input voltage: 0 V ± 0,1 V;

— High level input voltage: V_{DD} ± 0,1 V (AC series); 3 V ± 0,1 V (ACT series);

— Rise time of the input signal: $t_r \leq 5$ ns
(measured from 10 % to 90 % of the step amplitude);

— Fall time of the input signal: $t_f \leq 5$ ns
(measured from 90 % to 10 % of the step amplitude);

— Pulse repetition frequency: ≤ 5 MHz.