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INTERNATIONAL STANDARD

Printed boards and printed board assemblies – Design and use –
Part 5-4: Attachment (land/joint) considerations – Components with J leads on two sides

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International Standard IEC 61188-5-4 has been prepared by IEC technical committee 91: Electronics assembly technology

The text of this standard is based on the following documents:

FDIS	Report on voting
91/703/FDIS	91/735/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts of the IEC 61188 series, under the general title *Printed boards and printed board assemblies – Design and use*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

A bilingual version of this standard may be issued at a later date.

INTRODUCTION

This part of IEC 61188 covers land pattern for components with J leads on two sides.

The proposed land pattern dimensions in this standard are based upon the fundamental tolerance calculation combined with the given land protrusions and courtyard excesses (see IEC 61188-5-1, Generic requirements). The courtyard includes all issues of the normal manufacturing necessities.

The unaltered land pattern dimensions of this part are generally applicable for the solder paste application plus reflow soldering process. For application of the wave soldering process (though uncommon for SOJ components) the land pattern and courtyard dimensions may have to be modified. An orientation parallel to the wave direction is strongly recommended and suitably dimensioned solder thieves should be added.

This standard offers a threefold land pattern dimensioning (levels 1, 2, 3) on the basis of a threefold set of land protrusions and courtyard excesses: maximum (max.); medium (mdn); and minimum (min.). Nevertheless the user may develop deviating land pattern dimensions based upon the methodology of IEC 61188-5-1, introducing his own special material and assembling process conditions C, F, P and perhaps his own special land protrusions and courtyard excesses dimensions, as required.

If a user has good reasons to use a concept different from that of IEC 61188-5-1 or if the user prefers unusual land protrusions, this standard should be used for checking the resulting solder fillets.

It is the responsibility of the user to verify his used SMD land patterns for achieving an undisturbed mounting process including testing and an ensured reliability for the product stress conditions in use.

PRINTED BOARDS AND PRINTED BOARD ASSEMBLIES – DESIGN AND USE –

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1 Scope

This part of IEC 61188 provides the component and land pattern dimensions for small outline integrated circuits with "J" leads on two sides (SOJ components) used in the reflow soldering process. Basic construction of the SOJ device is also covered. Clause 4 lists the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60068-2-58, *Environmental testing – Part 2-58: Tests: Test Td. Test methods for solderability, resistance to dissolution of metallization and to soldering heat of surface mounting devices (SMD)*

IEC 60286-3, *Packaging of components for automatic handling – Part 3: Packaging of surface mount components on continuous tapes*

IEC 60286-4, *Packaging of components for automatic handling – Part 4: Stick magazines for electronic components encapsulated in packages of form E and G*

IEC 60286-5, *Packaging of components for automatic handling – Part 5: Matrix trays*

IEC 61760-1, *Surface mounting technology – Part 1: Standard method for the specification of surface mounting components (SMDs)*

3 General information

3.1 General component description

The two-sided J lead family is a small outline family identified by the dimensions of the body size in inches. For example, the SOJ/300 has a body size of 0,300 in or 7,63 mm, the SOJ/350 has a body size of 0,350 in or 8,88 mm, the SOJ/400 has a body size of 0,400 in or 10,12 mm, and the SOJ/450 has a body size of 0,450 in or 11,38 mm. Package lead counts range from 14 to 28 pins. Pitch is uniformly for all sizes, i.e. 1,27 mm.

The small-outline J (SOJ) package has leads on two sides, similar to a DIP. The lead configuration, like the letter J, extends out the side of the package and bends under the package forming a J bend. The point of contact of the lead to the land pattern is at the apex of the J bend and is the basis for the span of the land pattern.

The (inner) end of the J is called the heel, and the outer side of the J is called the toe.

The leads shall be coplanar within 0,1 mm. That is, when the component is placed on a flat surface, no lead may be more than 0,1 mm off the flat surface.

The SOJ package takes advantage of chips having parallel address or data line layouts. For example, memory ICs are often used in multiples, and bus lines connect to the same pin on each chip. Memory chips in SOJ packages can be placed close to one another because of the parallel pin layout and the use of J leads. With high capacity memory systems, the space savings can be significant compared with a dual in-line.

3.2 Marking

The marking of the SOIC family of parts shall comply with the definitions in the relevant IEC product specifications.

3.3 Packaging

Components may be provided in

- tape packaging: reference IEC 60286-3,
- stick magazine: reference IEC 60286-4,
- tray packaging: reference IEC 60286-5.

Bulk packaging is not recommended because of lead coplanarity conditions required for placement and soldering.

3.4 Process considerations

Together with other components assembled on PC boards, J lead packages are normally processed using standard solder reflow processes. Parts should therefore have an adequate solderability and resistance to soldering heat. These capabilities shall be demonstrated by submitting the parts to the test conditions of IEC 60068-2-58 and by complying with the conditions defined in IEC 61760-1.

The land pattern dimensions are based on a mathematical model that establishes a platform for a solder joint attachment to the printed board. The existing models create a platform that is capable of establishing a reliable solder joint no matter what the solder alloy used to make that joint (lead-free, tin lead, etc.).

Process requirements for solder reflow are different based on the solder alloy and should be analyzed in order that the process is above the liquidus temperature of the alloy, and remains above that temperature a sufficient time to form a reliable metallurgical bond.

4 Small outlined J packages (SOJ)

4.1 Component description

Figure 1 shows a typical construction example.

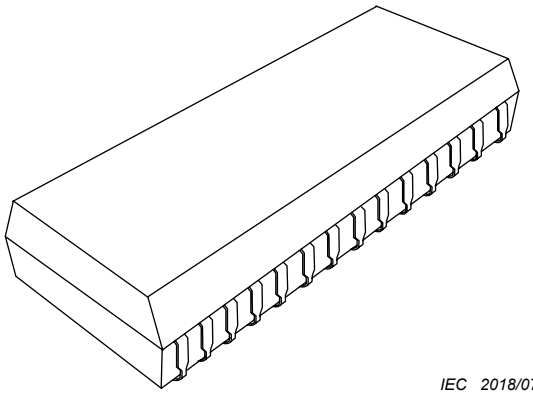
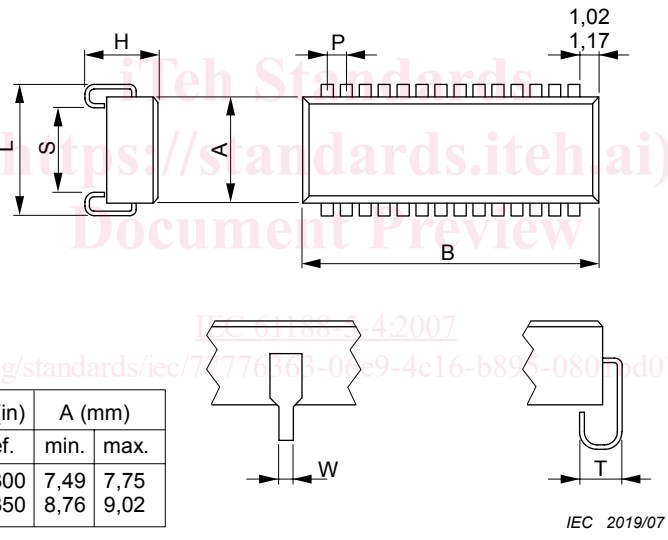


Figure 1 – SOJ construction

4.2 Component dimensions

Figure 2 shows the component dimensions for SOJ components.



A (in)	A (mm)	
ref.	min.	max.
0,300	7,49	7,75
0,350	8,76	9,02

Dimensions in millimetres