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SLOVENSKI STANDARD
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Mechanical standardization of semiconductor devices - Part 3: General rules for the preparation of outline drawings of integrated circuits (IEC 60191-3:1999)

Mechanical standardization of semiconductor devices -- Part 3: General rules for the preparation of outline drawings of integrated circuits

Mechanische Normung von Halbleiterbauelementen -- Teil 3: Allgemeine Regeln für die Erstellung von Gehäusezeichnungen für integrierte Schaltungen

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31.080.01	Polprevodniški elementi (naprave) na splošno	Semiconductor devices in general
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Mechanical standardization of semiconductor devices Part 3: General rules for the preparation of outline drawings of integrated circuits (IEC 60191-3:1999)

Normalisation mécanique des dispositifs à semiconducteurs
Partie 3: Règles générales pour la préparation des dessins d'encombrement des circuits intégrés
(CEI 60191-3:1999)

Mechanische Normung von Halbleiterbauelementen
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European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B - 1050 Brussels

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Foreword

The text of document 47D/299/FDIS, future edition 2 of IEC 60191-3, prepared by SC 47D, Mechanical standardization of semiconductor devices, of IEC TC 47, Semiconductor devices, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 60191-3 on 1999-10-01.

The following dates were fixed:

– latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement	(dop)	2000-07-01
– latest date by which the national standards conflicting with the EN have to be withdrawn	(dow)	2002-10-01

Annexes designated "normative" are part of the body of the standard.
Annexes designated "informative" are given for information only.
In this standard, annexes A, C, D, E, F, G, H, K and ZA are normative and annex B is informative.
Annex ZA has been added by CENELEC.

Endorsement notice

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Annex ZA (normative)

Normative references to international publications with their corresponding European publications

This European Standard incorporates by dated or undated reference, provisions from other publications. These normative references are cited at the appropriate places in the text and the publications are listed hereafter. For dated references, subsequent amendments to or revisions of any of these publications apply to this European Standard only when incorporated in it by amendment or revision. For undated references the latest edition of the publication referred to applies (including amendments).

NOTE: When an international publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

Publication	Year	Title	EN/HD	Year
IEC 60191-1	1966	Mechanical standardization of semiconductor devices Part 1: Preparation of drawings of semiconductor devices	-	-
IEC 60191-2	1995	Part 2: Dimensions	-	-
IEC 60191-4	1999	Part 4: Coding system and classification into forms of package outlines for semiconductor device packages	EN 60191-4	1999
ISO 1101-1	[1]	Geometrical Product Specification (GPS) Geometrical tolerancing - Generalities, definitions, symbols, indications on drawings	-	-
ISO 2692	1988	Technical drawings - Geometrical tolerancing - Maximum material principle	-	-

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Part 3:
General rules for the preparation of outline drawings of integrated circuits

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

Part 3: General rules for the preparation of outline drawings of integrated circuits

FOREWORD

1) The IEC (International Electrotechnical Commission) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of the IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, the IEC publishes International Standards. Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. The IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.

2) The formal decisions or agreements of the IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested National Committees.

3) The documents produced have the form of recommendations for international use and are published in the form of standards, technical reports or guides and they are accepted by the National Committees in that sense.

4) In order to promote international unification, IEC National Committees undertake to apply IEC International Standards transparently to the maximum extent possible in their national and regional standards. Any divergence between the IEC Standard and the corresponding national or regional standard shall be clearly indicated in the latter.

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International Standard IEC 60191-3 has been prepared by subcommittee 47D: Mechanical standardization of semiconductor devices, of IEC technical committee 47: Semiconductor devices.

This second edition cancels and replaces the first edition published in 1974, amendment 1 (1983), amendment 2 (1995), IEC 60191-3A (1976), IEC 60191-3B (1978), IEC 60191-3C (1987), IEC 60191-3D (1988), IEC 60191-3E (1990) and IEC 60191-3F (1994).

The text of this standard is based on the following documents:

FDIS	Report on voting
47D/299/FDIS	47D/322/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with ISO/IEC Directives, Part 3.

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Annexes A, C, D, E, F, G, H and K form an integral part of this standard.

Annex B is for information only.

The committee has decided that the contents of this publication will remain unchanged until 2005. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition; or
- amended.

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MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

Part 3: General rules for the preparation of outline drawings of integrated circuits

1 General

1.1 Scope

This part of IEC 60191 gives guidance on the preparation of drawings of integrated circuit outlines.

1.2 Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this part of IEC 60191. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this part of IEC 60191 are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies. Members of IEC and ISO maintain registers of currently valid International Standards.

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IEC 60191-1:1966, *Mechanical standardization of semiconductor devices – Part 1: Preparation of drawings of semiconductor devices*

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IEC 60191-2:1995, *Mechanical standardization of semiconductor devices – Part 2: Dimensions*

IEC 60191-4:1999, *Mechanical standardization of semiconductor devices – Part 4: Coding system and classification into forms of package outlines for semiconductor devices*

ISO 1101-1, — *Geometrical Product Specification (GPS) – Geometrical tolerancing – Generalities, definitions, symbols, indications on drawings* [1)]

ISO 2692:1988, *Technical drawings – Geometrical tolerancing – Maximum material principle*

2 Terminology and definitions

For the purpose of this part of IEC 60191, the following definitions apply.

2.1
package outline drawing
the drawing of a package which specifies the dimensional characteristics and other closely associated features which are required for mechanical interchangeability.

[1)] To be published.

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2.2
seating plane
a plane which designates the plane of contact of the package, including any stand-off, with the surface on which it will be mounted.

NOTE – This plane is often used as the reference plane.

2.3
base plane
a plane drawn parallel to the seating plane through the lowest point of the package, excluding any stand-off.

2.4
gauging plane
a plane perpendicular to the terminals, at which the position of the terminals is controlled.

NOTE – In some packages, two or more of the above-mentioned planes may coincide.

2.5
terminal position
one of a series or equally spaced locations on a circle or on a row, which may or may not be occupied by a terminal.

2.6
visual index
a reference feature (e.g. mark, chamfer, notch, tab, depression, etc.) which identifies the first terminal position.

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2.7
index area
the area in which a portion or all of the visual index should lie.

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2.8
mechanical index
a feature (e.g. tab, notch, flat, groove, etc.) which provides orientation during automatic handling.

Where possible, the mechanical index should coincide with the visual index.

2.9
index centre line or datum line
a centre line through a visual index feature (e.g. tab) which is used to orientate the index with the first terminal position.

2.10
grid reference corner
the first terminal position (viewed from the free end of the terminals) in an alphanumeric grid system.

2.11
terminal row
a series of equally spaced terminal positions which are located on a straight line.

2.12
terminal circle
a series of equally spaced terminal positions which are located on a circle.

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2.13
gauging zone
a control zone within which positional tolerances for the terminal axes or the planes of terminal symmetry are specified.

2.14
dambar
metal barrier extending between adjacent leads to restrict the flow of mold compound material between and along leads.

2.15
dambar protrusion
the presence of excess metal extending outward from the edge of a lead shoulder.

The width of the protrusion is the perpendicular distance from the defined lead edge to the outermost portion of the excess metal. The length of the protrusion is the largest dimension of the excess metal parallel to the defined lead edge (see figure 1a).

2.16
dambar intrusion
the absence of metal causing a discontinuity along the intended profile of a lead shoulder.

The depth of the intrusion is the perpendicular distance from the defined lead shoulder edge to the innermost edge of the region of absent metal. The length of the intrusion is the largest dimension of the region of absent metal parallel to the defined lead edge (see figure 1b).

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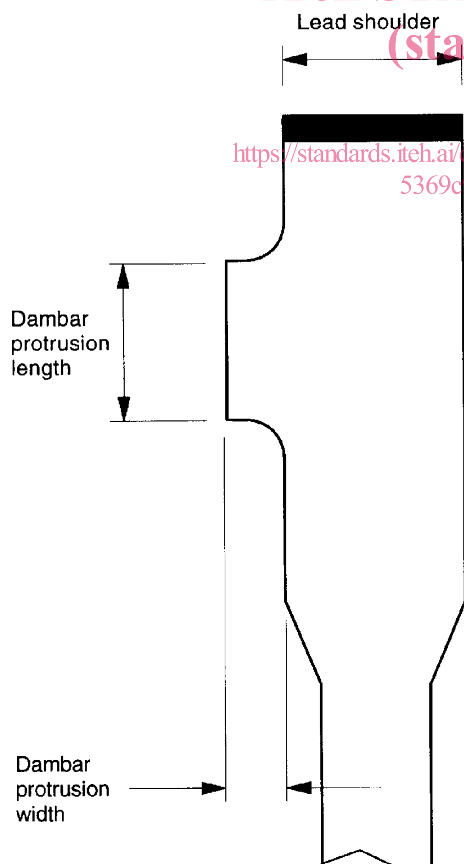

Figure 1a – Protrusion

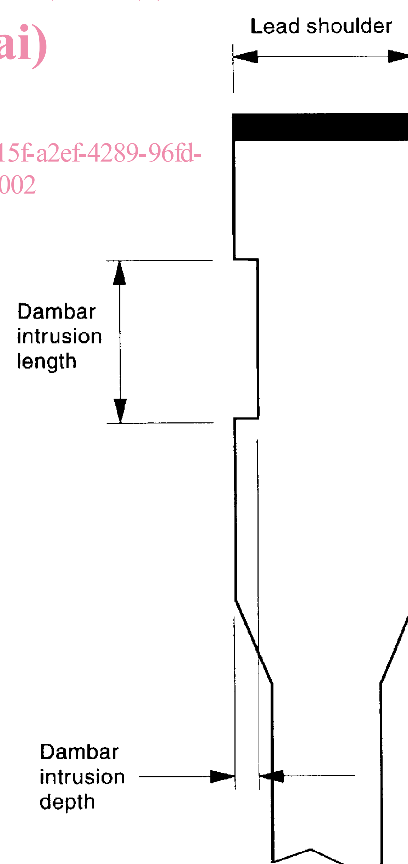

Figure 1b – Intrusion

Figure 1 – Dambar protrusion and intrusion

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2.17
mold flash
opaque mold compound material attached to the finished part and extending onto, between, and/or around adjacent leads and package edges.

2.18
interlead (window) flash
opaque mold compound material attached to an area between adjacent leads remaining after dambar trim operations.

2.19
protrusion
plastic or metal excess material remaining from the molding and trim/form/singulation operations.

2.20
gate burrs
excess metal material remaining after singulating the package from its leadframe at the mold gate area.

3 Cross-referencing of packages

The classification into forms of package outlines for semiconductor devices in IEC 60191-4 has superseded the form descriptions of forms 1 - 5 below. The cross-referencing to forms 1 - 5 is given for information purposes only.

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Cross-referencing is achieved by using the drawings in annex B as follows.

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3.1 Form 1 (axial) – figures B.1, B.2, B.3, B.4, B.5 and B.6

3.2 Form 2 (axial) – figures B.7, B.7a, B.8 and B.9

3.3 Form 3 (axial) – figures B.10, B.11 and B.12

3.4 Form 4 (peripheral) – figures B.13, B.14, B.15, B.16, B.16a, B.17 and B.18

3.5 Form 5 (special)

This form, for which there are no examples given in annex B, refers to figures which are combinations of axial and peripheral or which, for other reasons, e.g. leadless packages, do not fit in the axial or peripheral categories.

4 Terminal identification – Numbering of terminals

Where possible, device terminals should be identified according to the following rules.

4.1 Devices with terminals disposed in linear array (see figure B.2)

The terminals are considered as being viewed from their free ends. The terminal nearest the visual index should be numbered as No. 1, the other terminals should be numbered progressively from terminal No. 1.

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4.2 Devices with terminals disposed on a single circular array (see figures B.10 and B.11)

The terminals are considered as being viewed from their free ends. The terminal, the centre of which is past the datum line of the visual index should be numbered as No. 1, the other terminals should be numbered progressively in a clockwise sequence from terminal No. 1.

Where omission of one terminal in an otherwise equally spaced array identifies the datum line, the position of the omitted terminal should not be numbered; but in a fixed modular circuit array, any location of omitted terminal which does not define a datum line shall be numbered.

4.3 Devices with terminals disposed on multiple circular arrays (see figure B.12)

The rules given in 4.2 will be applied as follows: the terminals located on the pitch circle of the largest diameter should be numbered A1, A2, A3, etc., the terminals located on the other pitch circles of decreasing diameter should be numbered progressively B1, B2, B3, etc., C1, C2, C3, etc.

4.4 Devices with terminals disposed on a square or rectangular periphery (see figures B.1, B.3, B.4, B.6, B.7, B.7a, B.8, B.9, B.13, B.14, B.25, B.16, B.16a, B.17 and B.18)

Visual identification of the top of the device should be provided. The means of identification of terminal position No. 1 should also be provided. These identifications may be combined.

When terminal No. 1 marking is required on the bottom side of the package, the following convention is used (see figures H.1 and H.2).

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The terminal positions should be numbered progressively in an anti-clockwise direction around the periphery of the device as viewed from the top. The terminal position No. 1 shall be the first position anti-clockwise from the means of identification.

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Each terminal shall be identified by the number of its position. Terminals may not necessarily be present in all the numbered positions, but those present shall have the number of the position.

When a terminal occupies more than one terminal position, this terminal should be identified by the number of the first and last occupied terminal positions, these two numbers being separated by a dash.

(For a theoretical example, see figure 2.)

When the device presents more than two rows of terminals in one direction, because the folding of the terminals emerging in one plane has been made in more than two planes, the terminals should be numbered progressively in correspondence with the position of their point of emergence from the body of the device.

(For a theoretical example, see figure 3.)