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First edition
2007-02

Logic digital integrated circuits – Specification for I/O interface model for integrated circuit (IMIC version 1.3)

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

LOGIC DIGITAL INTEGRATED CIRCUITS – SPECIFICATION FOR I/O INTERFACE MODEL FOR INTEGRATED CIRCUIT (IMIC version 1.3)

FOREWORD

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- the subject is still under technical development or where, for any other reason, there is the future but no immediate possibility of an agreement on an International Standard.

Technical specifications are subject to review within three years of publication to decide whether they can be transformed into International Standards.

IEC 62404, which is a technical specification, has been prepared by subcommittee 47A: Integrated circuits, of IEC technical committee 47: Semiconductor devices.

The text of this technical specification is based on the following documents:

Enquiry draft	Report on voting
47A/746/DTS	47A/751/RVC

Full information on the voting for the approval of this technical specification can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A bilingual version of this publication may be issued at a later date.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- transformed into an International standard,
- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

INTRODUCTION

With an increase in speed of electronic systems, it becomes necessary to accurately predict electrical performance including noise in electronic systems with integrated circuits.

Simulators have been used for this purpose. Simulators need accurate models for describing electrical properties of integrated circuits. Semiconductor manufacturers and/or suppliers are required by their users to prepare device models for various simulation tools, some of which are not compatible with SPICE. In addition, since SPICE models contain proprietary process parameters, a non-disclosure agreement is typically required to obtain these from the vendor.

IBIS (I/O Buffer Interface Specification) has been proposed as a model for integrated circuits, which, approved as IEC 62014-1, has the following features:

- since electrical properties of I/O buffers are described in table format, disclosure of proprietary information such as process parameters is drastically reduced;
- it is easy to get IBIS models that are supported by many simulation tools;
- a public domain tool can convert SPICE models into IBIS models.

However, IBIS models seem to have the following problems:

- the modeling of power and ground currents is insufficient for accurate power and ground bounce analysis;
- since an IBIS model has only the final stage at output and input, it is difficult to model the effect of loading on circuit boards on output and input waveforms. The fixed model taken by IBIS has little flexibility for describing other circuitry;
- in order to simulate EMI with accuracy, more information such as material constant and three-dimensional structures is needed.

LOGIC DIGITAL INTEGRATED CIRCUITS – SPECIFICATION FOR I/O INTERFACE MODEL FOR INTEGRATED CIRCUIT (IMIC version 1.3)

1 Scope

The following items are considered to standardize the electrical modeling of input signals, output signals, power supply and ground terminals of integrated circuits, in order to provide for analysis of electrical characteristics of equipment.

1) To standardize in order to solve current problems and in order to extend capabilities of analysis, on the basis of results of the past standardization activities.
2) To define more flexible description rules for electric circuits in order to provide more accurate analysis of printed circuit board.
3) To introduce the concept of modeling levels to exchange relevant data for each application.
4) To enhance electrical modeling for packages and modules.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 62014-1:2001, *Electronic design automation libraries – Part 1: Input/output buffer information specifications (IBIS version 3.2)*

3 Terms and definitions

Under consideration

4 Outline

4.1 General

The outline of this model is shown in Figure 1.

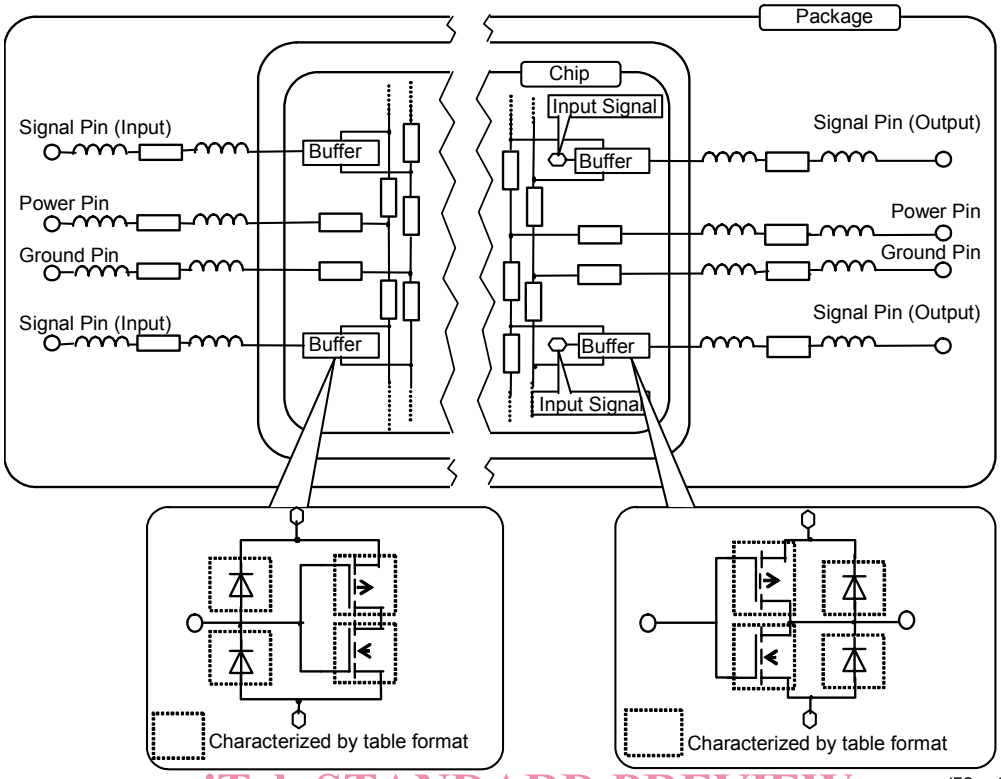

Figure 1 – Outline of the model

4.2 Covered range of model

The model is described as circuits covering the whole or a part of the I/0 buffers and the package.

4.3 Language for circuits

The circuits shall be described in extended SPICE format. The structure allows describing simple buffers, complex buffers, power and ground lines, packages and complex memory module boards in a unified format.

4.4 Device model

The characteristics of non-linear devices redescribed in one-dimensional, two-dimensional or three-dimensional table format.

4.5 Structure of model

The data of the model consists of integrated circuit, package and module portions. Therefore each portion can be generated independently.

4.6 Simulation

The netlist of printed circuit board and the I/O buffer model defined by this specification provides accurate circuit simulation results.

4.7 Relation to IBIS

Tools that can extract IBIS data from this model are possible to develop.

5 Model structure

The model shall describe the inside of ICs, packages and module boards as shown in Figure 2.

The models of IC, package and module board consist of the elements given in Table 1.

The data structures of IC, package and module board models are shown in Figure 3, Figure 4, and Figure 5, respectively.

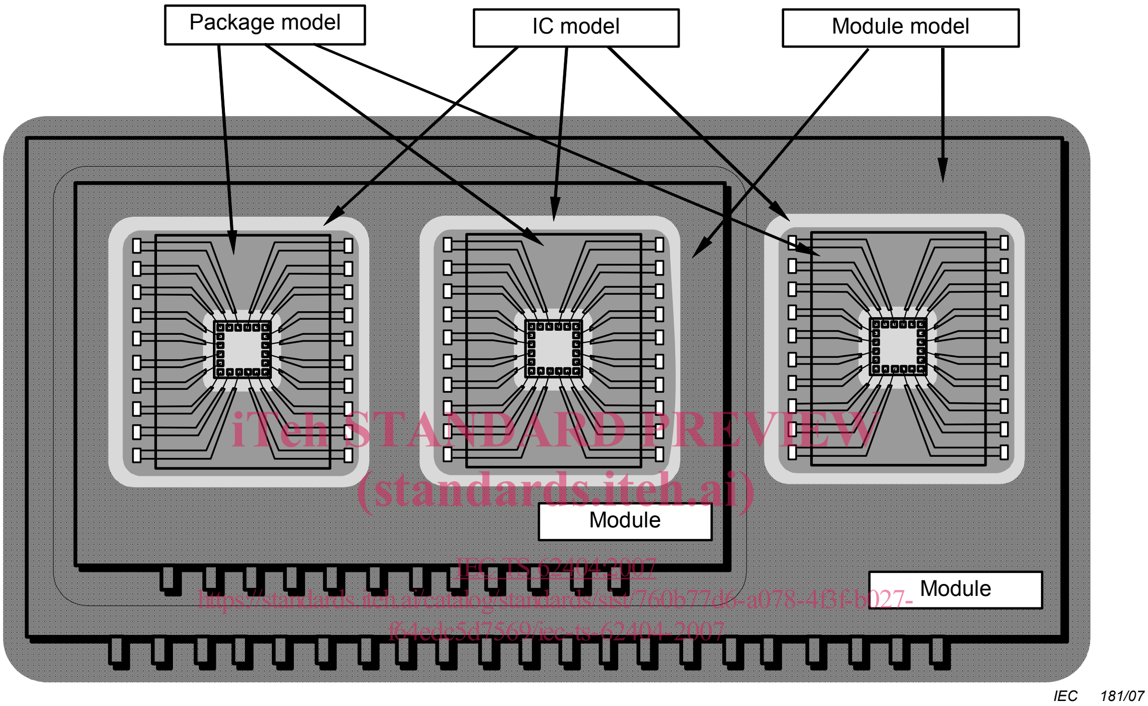

Figure 2 – Hierarchy of three models

Table 1 – Elements of model structures

File	Element	Description
IC model file	Header	IC type, model version, model level.
	External terminals	IC external terminals (package pins).
	Pad assignment	Connection between IC pads and package inner terminals.
	Circuit description	Internal circuits and their connections.
	Input stimulus assignment	Internal circuits and their stimuli to generate output waveforms.
	Input stimulus	Input waveforms.
	Device model	Characteristics of non-linear circuits in one-dimensional, two-dimensional and three-dimensional table data. Non-linear devices are transistors, diodes and so on.
	Package model reference	Name of the package model to be used.
Package model file	Header	Package name, model version, model level.
	Model name	List of models in package circuit model.
	Inner terminal	Cross-reference between internal terminals and package internal circuit model.
	Outer terminal	Cross-reference between external circuit and package internal circuit model.
	Circuit description	Internal circuits and their connections.
	Device model	Characteristics of non-linear circuits in one-dimensional, two-dimensional and three-dimensional table data. Non-linear devices are transistors, diodes and so on.
	Structure	Material, position, three-dimensional structures.
Module model file	Header	Module name, model version, model level.
	External terminals	External terminals (pins) of module.
	Circuit description	Internal circuits and their connections.
	Signal source	Internal circuits and their terminals to generate output waveforms at corresponding external terminals.
	Device model	Characteristics of non-linear circuits in one-dimensional, two-dimensional and three-dimensional table data. Non-linear devices are transistors, diodes and so on.
	IC/Module model reference	Names of IC/module model files and model names to be used.
	Structure	Material, position, three-dimensional structures.

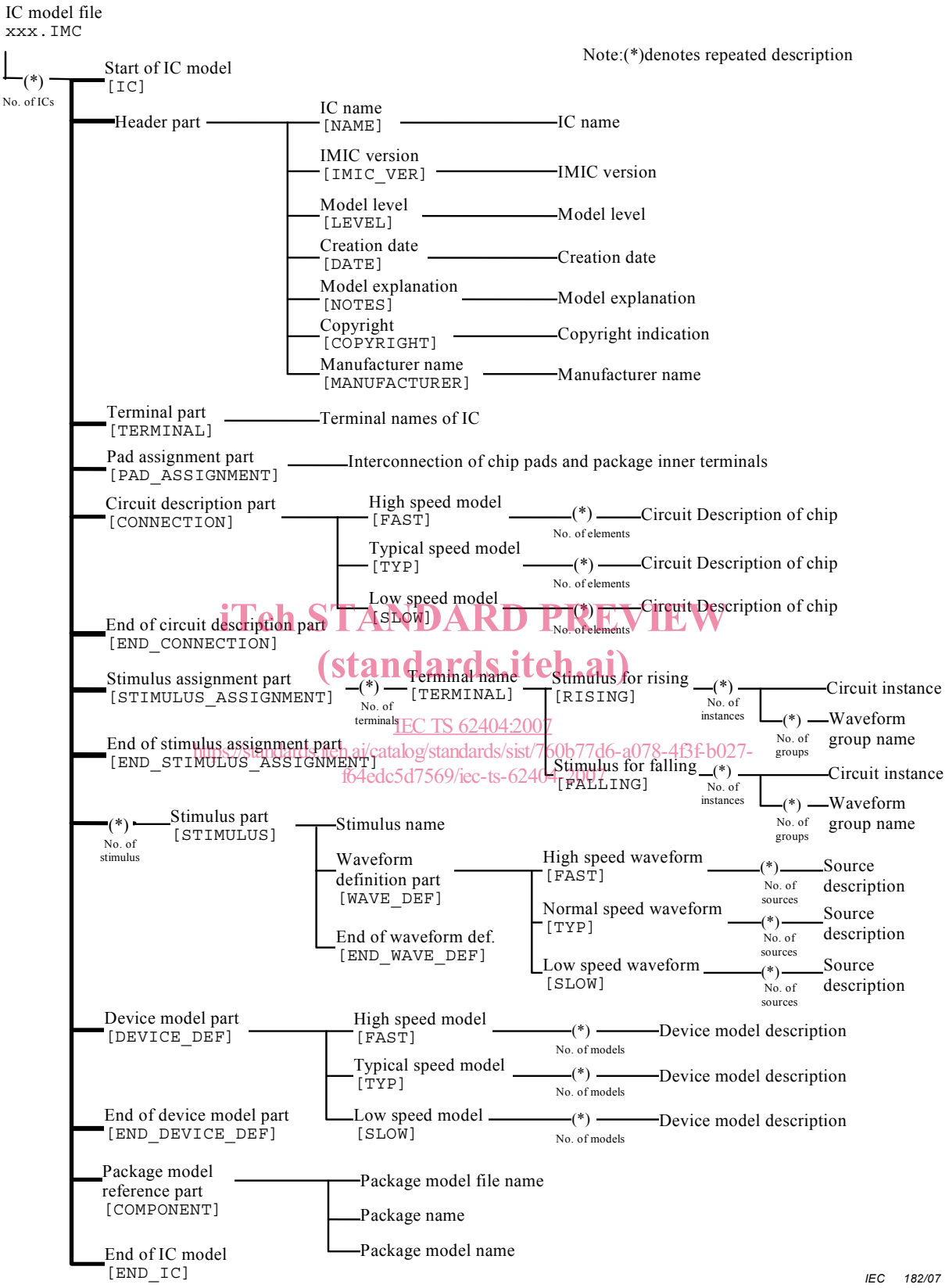

Figure 3 – Data structure of an IMIC model file for IC

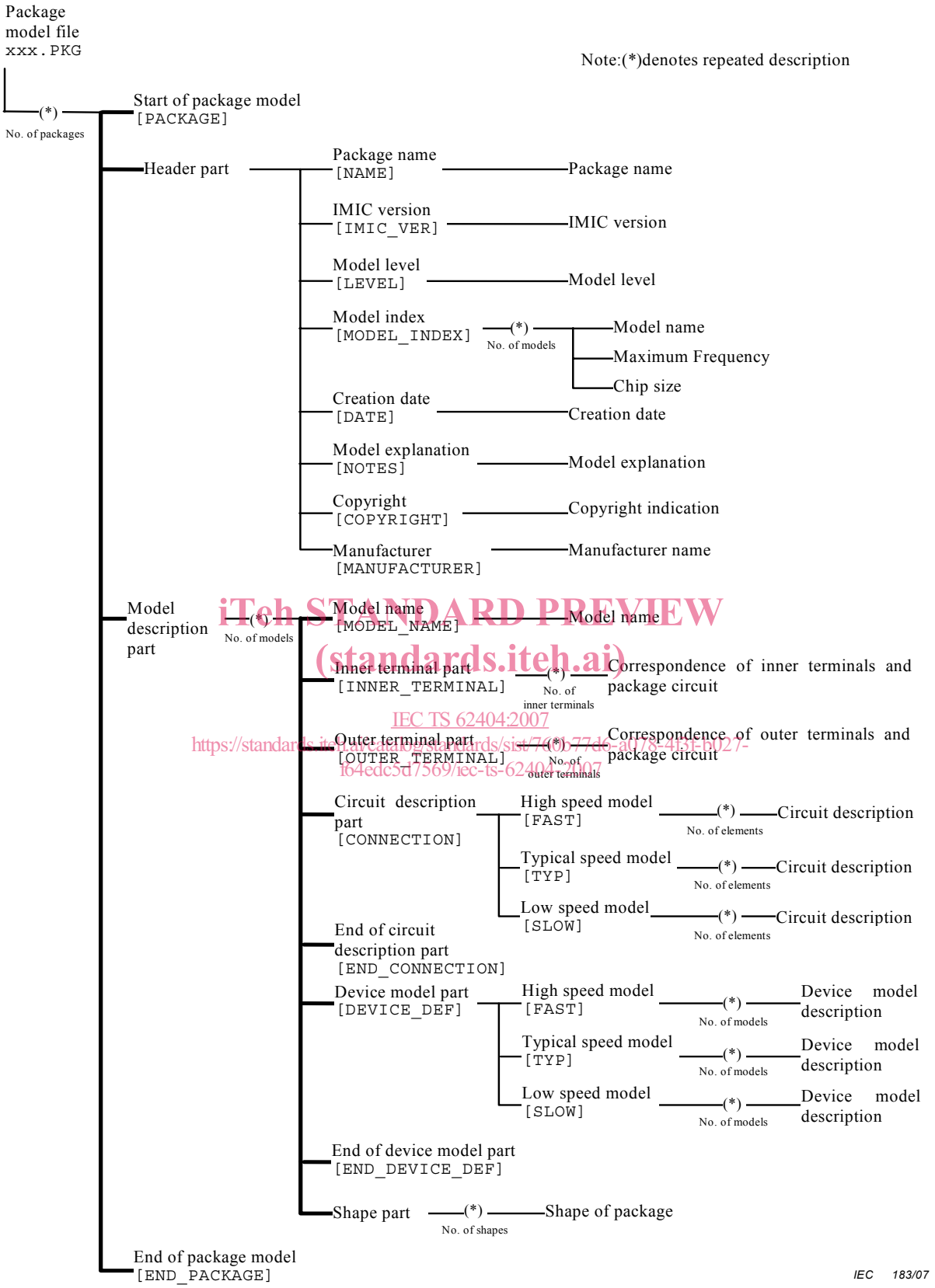

Figure 4 – Data structure of an IMIC model file for package

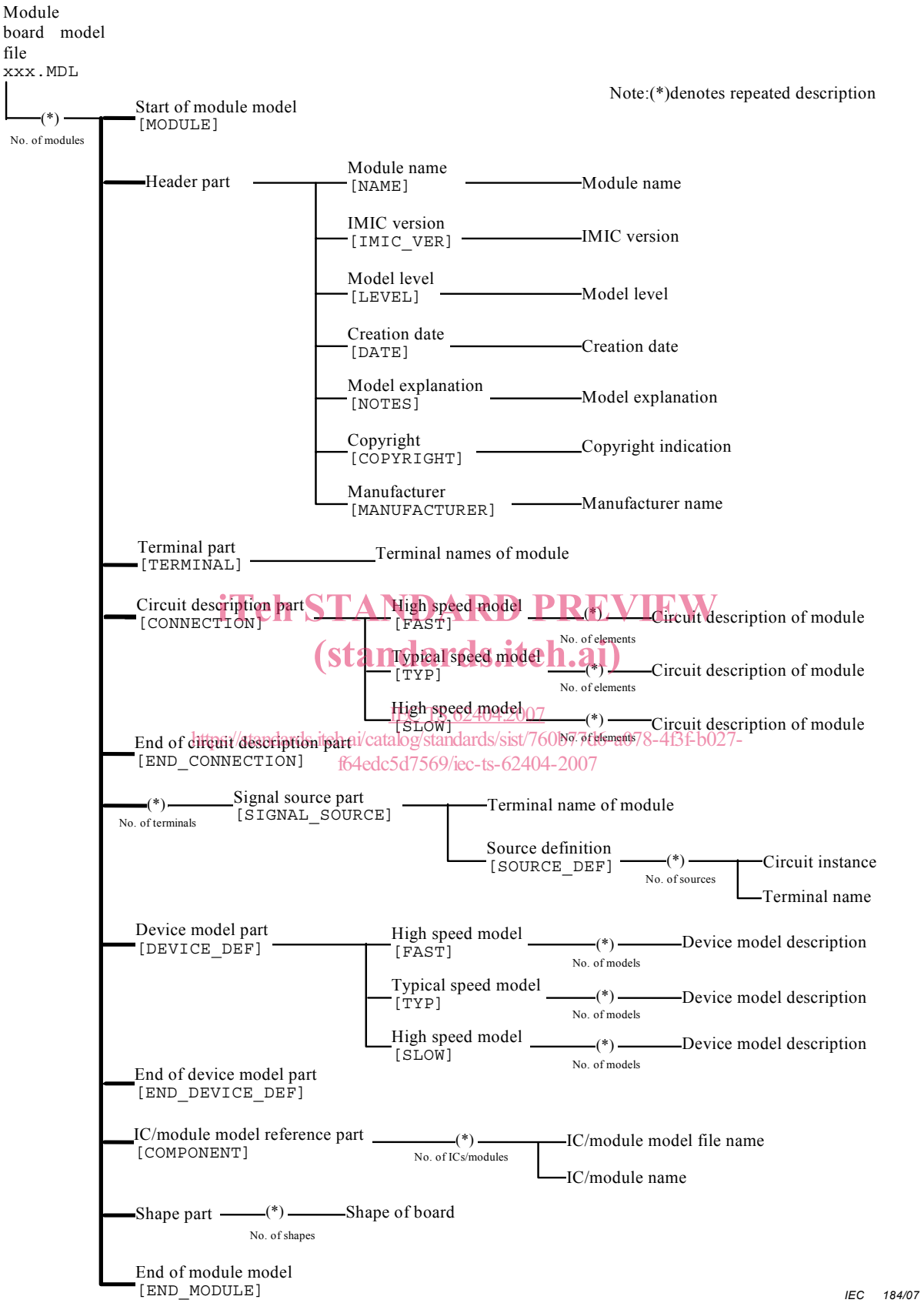

Figure 5 – Data structure of an IMIC model file for module