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TECHNICAL SPECIFICATION

Integrated circuits – Measurement of impulse immunity –
Part 2: Synchronous transient injection method

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CONTENTS

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Part 2: Synchronous transient injection method

FOREWORD

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Technical specifications are subject to review within three years of publication to decide whether they can be transformed into International Standards.

IEC 62215-2, which is a technical specification, has been prepared by subcommittee 47A: Integrated circuits, of IEC technical committee 47: Semiconductor devices.

The text of this technical specification is based on the following documents:

Enquiry draft	Report on voting
47A/762/DTS	47A/769A/RVC

Full information on the voting for the approval of this technical specification can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all the parts in the IEC 62215 series, under the general title *Integrated circuits – Measurement of impulse immunity*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- transformed into an International standard,
- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

INTRODUCTION

In future standards, test methods and measurement procedures will be given for transient immunity of integrated circuits:

– ESD pulse with resemblance to IEC 61000-4-2;
– EFT pulse with resemblance to IEC 61000-4-4;
– Surge pulse with resemblance to IEC 61000-4-5.

INTEGRATED CIRCUITS – MEASUREMENT OF IMPULSE IMMUNITY –

Part 2: Synchronous transient injection method

1 Scope

IEC/TS 62215-2, which is a technical specification, contains general information and definitions on the test method to evaluate the immunity of integrated circuits (ICs) against fast conducted synchronous transient disturbances. This information is followed by a description of measurement conditions, test equipment and test set-up as well as the test procedures and the requirements on the content of the test report.

The objective of this technical specification is to describe general conditions to obtain a quantitative measure of immunity of ICs establishing a uniform testing environment. Critical parameters that are expected to influence the test results are described. Deviations from this specification should be explicitly noted in the individual test report.

This synchronous transient immunity measurement method, as described in this specification, uses short impulses with fast rise times of different amplitude, duration and polarity in a conductive mode to the IC. In this method, the applied impulse should be synchronized with the activity of the IC to make sure that controlled and reproducible conditions can be assured.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61967-4, *Integrated circuits – Measurement of electromagnetic emissions, 150 kHz to 1 GHz – Part 4: Measurement of conducted emissions – 1 Ω/150 Ω direct coupling method*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 62215-1 (in preparation), as well as the following, apply.

3.1
auxiliary equipment
AE
equipment not under test that is nevertheless indispensable for setting up all the functions and assessing the correct performance (operation) of the equipment under test (EUT) during its exposure to the disturbance

3.2
coupling network
electrical circuit for transferring energy from one circuit to another with well-defined impedance and known transfer characteristics

3.3
device under test
DUT
device, equipment or system being evaluated

NOTE In this technical specification, it refers to a semiconductor device being tested.

3.4
electromagnetic compatibility
EMC
ability of an equipment or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbance to anything in that environment

[IEC 60050(161):1990, definition 161-01-07]

3.5
electrical noise
unwanted electrical signals, which produce undesirable effects in the circuits of the control system in which they occur

[IEEE std 100-1992-518-1982]

3.6
immunity (to a disturbance)
ability of a device, equipment or system to perform without degradation in the presence of an electromagnetic disturbance

3.7
jitter (time related)
short-term variations of the significant instants of a digital signal from their ideal positions in time

3.8
RF ambient
totality of electromagnetic phenomena existing at a given location

3.9
transient
pertaining to or designating a phenomenon or a quantity which varies between two consecutive steady states during a time interval which is short compared with the time-scale of interest

[IEC 60050(161):1990, definition 161-02-01]

4 General

4.1 Introduction

This immunity test method describes synchronous transient injection on digital and mixed-signal ICs. In this method an impulse is injected into the V_{ss}-, V_{dd}-pin(s) or I/Os successively on the IC subjected to the test.

4.2 Measurement philosophy

This method is related to the 1 Ω resistor method, see IEC 61967-4. In this method a 1 Ω resistor is added in series with the V_{dd}, V_{ss} pin(s) of the IC. It is assumed that the voltage drop across the 1 Ω resistor in parallel with the DC by-pass inductance is very small. For injecting the impulse, a broadband coupling network is defined. The impulse injection is synchronized to a program loop signal generated by the IC.

One cycle of this response signal is considered as one program loop. The aim of this measurement method is to insert a synchronous but delayed impulse into the IC, related to the program loop. The total time of one program loop period is calculated and then it is

divided into small time steps. At every delay step, a single impulse per program loop is inserted into the IC and its response is measured.

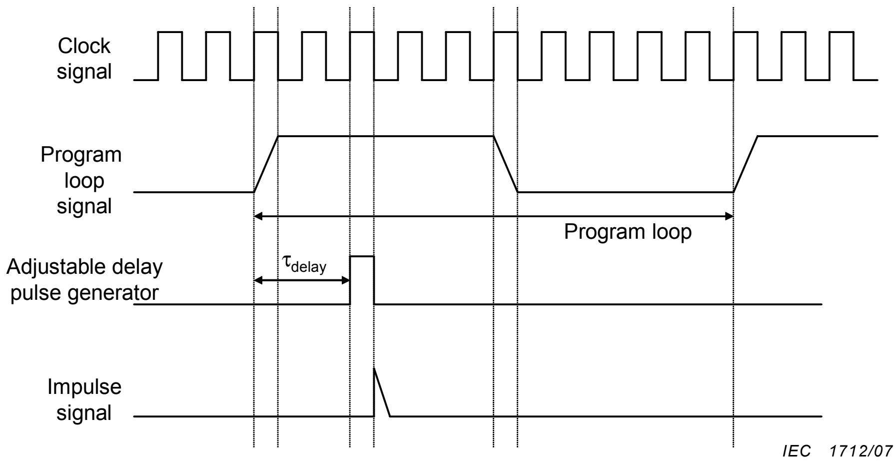

Figure 1 – Synchronous transient injection immunity methodology waveforms

Figure 1 shows the relevant signals occurring in this synchronous transient immunity test. The clock signal is used to run the digital IC and the program loop signal is used as a reference and response signal. A predetermined adjustable delay is used to shift the impulse delay time; τ_{delay}, along the program loop.; τ_{delay} is typically a fraction (≤ 0,1) of the rise time of the clock signal. The rising edge of the program loop signal, synchronized with the rising edge of the clock signal, is considered as a fixed reference point, see Figure 1, second line; program loop sync circuitry. Thereafter, the impulse is inserted and the edges of the response signals have to be observed. After every program loop, the delay step is increased and the injection moment of the impulse is shifted. In this way, the full scan can be completed through the program cycle to evaluate the impulse immunity.

The test method will show sensitive time windows, i.e. modes of operation at which the device is sensitive. The non-sensitive time windows can be skipped thereafter while repeating the measurements.

NOTE This measurement methodology is different from to the stochastic i.e. random application of impulses.

4.3 Set-up concept

In Figure 2, the block diagram of the test set-up for the synchronous impulse immunity test is given. A trigger signal, e.g. generated by the DUT, is used as an indication to start the measurement. This signal is also used to trigger the delay pulse generator to produce the programmable delay. The delayed pulse triggers the impulse generator that produces an impulse. This impulse is then inserted into the DUT through a suitable coupling network. Measurement equipment such as an oscilloscope or time domain analyser is used to measure the response of the DUT versus the delay of the impulse in the program loop. This measuring equipment is also synchronized with the test signal to acquire the response data over a program loop. A computer interface is used to control the measurement test set-up and to acquire the response data from the test set-up.

In general, the test set-up shall be in accordance with the specific test procedure as described in the future IEC 62215-1. All the test relevant parameters shall be recorded as exactly as possible to ensure that the test results become reproducible.

4.4 Response signal

The response signal is a signal generated by the IC under test (DUT). A clock signal may be externally provided. If the DUT is a microcontroller, then the response signal can be

generated by a microcontroller by loading a small software program. If DUT is a logic device, then the output signal of the logic device is considered as the response signal. The immunity can be quantified based on jitter occurring in the response signal (or any other errors) due to the impulse disturbances applied.

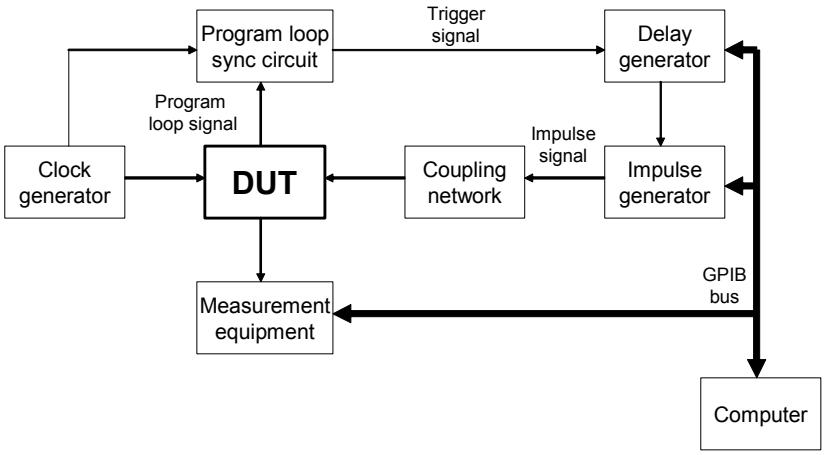

Figure 2 – Test set-up diagram for synchronous transient injection immunity testing

4.5 Coupling networks

4.5.1 General

The coupling network will always introduce a time delay for the applied impulse signal since a network presents a path (line) of a certain physical length for the signal.

4.5.2 Design of coupling networks

For synchronous transient immunity testing, it is important that the coupling networks have a flat transfer characteristics over a broad frequency range. This flatness will help to couple the impulse to the DUT without disturbing its impulse characteristics and will maintain the normal operating conditions of the DUT. The coupling networks are designed in such a way that the impulses of different amplitude, duration, rise and fall time can be injected into the DUT ports.

4.5.3 Coupling network for the ground/ V_{ss} pin(s)

The principle used to couple the impulse into the ground/ V_{ss} pin(s) is via a 1 Ω resistor connected in series with a ground pin(s) of the IC and where the impulse signal is applied in series equivalently. Figure 3 shows an example of a coupling network.

Two 4:1 transmission line (Guanella) transformers are used. A resistor network follows these two transformers together with an RF choke. When the two TL (transmission line) transformers having impedance ratio 4:1 are connected in series, it results in an impedance step down from 50 Ω to about 3 Ω. The resistor network of 3 Ω is connected as an RF load. To minimize the DC voltage drop across the 1 Ω resistor, an RF choke of 10 µH is connected in parallel. This inductor acts as a DC short-circuit and represents high impedance for the impulse signal which is referred to a parallel impedance of 1 Ω. The overall attenuation in the coupling network is approximately 22 dB; 6 dB attenuation by each transformer and 10 dB by the resistive network.