



SLOVENSKI STANDARD

SIST EN 61188-5-6:2003

01-november-2003

Printed boards and printed board assemblies - Design and use - Part 5-6: Attachment (land/joint) considerations - Chip carriers with J-leads on four sides

Printed boards and printed board assemblies - Design and use -- Part 5-6: Attachment (land/joint) considerations - Chip carriers with J-leads on four sides

Leiterplatten und Flachbaugruppen - Konstruktion und Anwendung -- Teil 5-6:
Betrachtungen zur Montage (Anschlussfläche/Verbindung) - Bauelemente mit J-förmigen
Anschlüssen auf vier Seiten

(standards.iteh.ai)

Cartes imprimées et cartes imprimées équipées - Conception et utilisation -- Partie 5-6:
Considérations sur les liaisons pistes-soudures - Composants à sorties en J sur quatre
côtés

Ta slovenski standard je istoveten z: EN 61188-5-6:2003

ICS:

31.180 Tiskana vezja (TIV) in tiskane Printed circuits and boards
plošče

SIST EN 61188-5-6:2003

en

iTeh STANDARD PREVIEW
(standards.iteh.ai)

[SIST EN 61188-5-6:2003](#)

<https://standards.iteh.ai/catalog/standards/sist/4eb05737-ac2b-469e-b933-454200a6bbe2/sist-en-61188-5-6-2003>

EUROPEAN STANDARD

EN 61188-5-6

NORME EUROPÉENNE

EUROPÄISCHE NORM

April 2003

ICS 31.190

English version

**Printed boards and printed board assemblies –
Design and use
Part 5-6: Attachment (land/joint) considerations –
Chip carriers with J-leads on four sides
(IEC 61188-5-6:2003)**

Cartes imprimées et cartes imprimées
équipées –

Conception et utilisation

Partie 5-6: Considérations sur les liaisons

pistes-soudures –

Composants à sorties en J sur quatre

côtés

(CEI 61188-5-6:2003)

Leiterplatten und Flachbaugruppen -
Konstruktion und Anwendung

Teil 5-6: Betrachtungen zur Montage

(Anschlussfläche/Verbindung) -

Bauelemente mit J-förmigen Anschlüssen

auf vier Seiten

(IEC 61188-5-6:2003)

iTeH STANDARD PREVIEW
(standards.iteh.ai)
<https://standards.iteh.ai/catalog/standards/sist/4eb05737-ac2b-469e-b933-454200a6bbe2/sist-en-61188-5-6-2003>

This European Standard was approved by CENELEC on 2003-03-01. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the Central Secretariat or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the Central Secretariat has the same status as the official versions.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Czech Republic, Denmark, Finland, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Luxembourg, Malta, Netherlands, Norway, Portugal, Slovakia, Spain, Sweden, Switzerland and United Kingdom.

CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B - 1050 Brussels

Foreword

The text of document 91/338/FDIS, future edition 1 of IEC 61188-5-6, prepared by IEC TC 91, Electronics assembly technology, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 61188-5-6 on 2003-03-01.

This European Standard should be read in conjunction with EN 61188-5-1:2002.

The following dates were fixed:

- latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 2003-12-01
- latest date by which the national standards conflicting with the EN have to be withdrawn (dow) 2006-03-01

Annexes designated "normative" are part of the body of the standard.
In this standard, annex ZA is normative.
Annex ZA has been added by CENELEC.

iTeh STANDARD PREVIEW

Endorsement notice (standards.iteh.ai)

The text of the International Standard IEC 61188-5-6:2003 was approved by CENELEC as a European Standard without any modification.

<https://standards.iteh.ai/catalog/standards/sist/4eb05737-ac2b-469e-b933-454200a6bbe2/sist-en-61188-5-6-2003>

Annex ZA (normative)

Normative references to international publications with their corresponding European publications

This European Standard incorporates by dated or undated reference, provisions from other publications. These normative references are cited at the appropriate places in the text and the publications are listed hereafter. For dated references, subsequent amendments to or revisions of any of these publications apply to this European Standard only when incorporated in it by amendment or revision. For undated references the latest edition of the publication referred to applies (including amendments).

NOTE When an international publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

<u>Publication</u>	<u>Year</u>	<u>Title</u>	<u>EN/HD</u>	<u>Year</u>
IEC 60068-2-58	- ¹⁾	Environmental testing Part 2-58: Tests - Test Td: Test methods for solderability, resistance to dissolution of metallization and to soldering heat of surface mounting devices (SMD)	EN 60068-2-58	1999 ²⁾
IEC 60191-2	- ¹⁾	Mechanical standardization of semiconductor devices Part 2: Dimensions	-	-
IEC 61188-5-1	- ¹⁾	Printed boards and printed board assemblies - Design and use Part 5-1: Attachment (land/joint) considerations - Generic requirements	EN 61188-5-1	2002 ²⁾
IEC 61760-1	- ¹⁾	Surface mounting technology Part 1: Standard method for the specification of surface mounting components (SMDs)	EN 61760-1	1998 ²⁾

1) Undated reference.

2) Valid edition at date of issue.

iTeh STANDARD PREVIEW
(standards.iteh.ai)

[SIST EN 61188-5-6:2003](#)

<https://standards.iteh.ai/catalog/standards/sist/4eb05737-ac2b-469e-b933-454200a6bbe2/sist-en-61188-5-6-2003>

**NORME
INTERNATIONALE
INTERNATIONAL
STANDARD**

**CEI
IEC**

61188-5-6

Première édition
First edition
2003-01

**Cartes imprimées et cartes imprimées équipées –
Conception et utilisation –**

**Partie 5-6:
Considérations sur les liaisons pistes-soudures –
Composants à sorties en J sur quatre côtés**

(standards.iteh.ai)

**Printed boards and printed board assemblies –
Design and use –**

SIST EN 61188-5-6:2003
<https://standards.iteh.ai/catalog/standards/sist/4eb05737-ac2b-469e-b933-454200a6bbe2/sist-en-61188-5-6-2003>

**Part 5-6:
Attachment (land/joint) considerations –
Chip carriers with J-leads on four sides**

© IEC 2003 Droits de reproduction réservés — Copyright - all rights reserved

Aucune partie de cette publication ne peut être reproduite ni utilisée sous quelque forme que ce soit et par aucun procédé, électronique ou mécanique, y compris la photocopie et les microfilms, sans l'accord écrit de l'éditeur.

No part of this publication may be reproduced or utilized in any form or by any means, electronic or mechanical, including photocopying and microfilm, without permission in writing from the publisher.

International Electrotechnical Commission, 3, rue de Varembe, PO Box 131, CH-1211 Geneva 20, Switzerland
Telephone: +41 22 919 02 11 Telefax: +41 22 919 03 00 E-mail: inmail@iec.ch Web: www.iec.ch



Commission Electrotechnique Internationale
International Electrotechnical Commission
Международная Электротехническая Комиссия

CODE PRIX
PRICE CODE

R

*Pour prix, voir catalogue en vigueur
For price, see current catalogue*

CONTENTS

FOREWORD	5
INTRODUCTION	9
1 Scope and object	11
2 Normative references.....	11
3 General information	13
3.1 General component description	13
3.2 Marking	13
3.3 Carrier packaging format	13
3.4 Process considerations.....	13
4 QFJ (square)	13
4.1 Introductory remark	13
4.2 Component description	13
4.3 Component dimensions	17
4.4 Solder joint fillet design	17
4.5 Land pattern dimensions.....	21
5 QFJ (rectangular)	25
5.1 Introductory remark	25
5.2 Component description	25
5.3 Component dimensions	27
5.4 Solder joint fillet design	29
5.5 Land pattern dimensions.....	33
Bibliography.....	37
Figure 1 – QFJ (square)	15
Figure 2 – QFJ (square) dimensions	17
Figure 3 – Solder joint fillet design of QFJ square component with different levels (see IEC 61188-5-1, Table 5)	21
Figure 4 – QFJ (square) land pattern dimensions	25
Figure 5 – QFJ (rectangular)	25
Figure 6 – QFJ (rectangular) dimensions.....	29
Figure 7 – Solder joint fillet design of QFJ rectangular component with different levels (see IEC 61188-5-1, Table 5)	33
Figure 8 – QFJ (rectangular) land pattern dimensions	35

INTERNATIONAL ELECTROTECHNICAL COMMISSION

**PRINTED BOARDS AND PRINTED BOARD ASSEMBLIES –
DESIGN AND USE –**
**Part 5-6: Attachment (land/joint) considerations –
Chip carriers with J-leads on four sides**

FOREWORD

- 1) The IEC (International Electrotechnical Commission) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of the IEC is to promote international cooperation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, the IEC publishes International Standards. Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. The IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
- 2) The formal decisions or agreements of the IEC on technical matters express, as nearly as possible, an international consensus of opinion on relevant subjects since each technical committee has representation from all interested National Committees.
- 3) The documents produced have the form of recommendations for international use and are published in the form of standards, technical specifications, technical reports or guides and they are accepted by the National Committees in that sense.
- 4) In order to promote international unification, IEC National Committees undertake to apply IEC International Standards transparently to the maximum extent possible in their national and regional standards. Any divergence between the IEC Standard and the corresponding national or regional standard shall be clearly indicated in the latter.
- 5) The IEC provides no marking procedure to indicate its approval and cannot be rendered responsible for any equipment declared to be in conformity with one of its standards.
- 6) Attention is drawn to the possibility that some of the elements of this International Standard may be the subject of patent rights. The IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 61188-5-6 has been prepared by IEC technical committee 91: Electronics assembly technology.

The text of this standard is based on the following documents:

FDIS	Report on voting
91/338/FDIS	91/366/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

IEC 61188-5-6 should be read in conjunction with IEC 61188-5-1.

IEC 61188-5 consists of the following parts, under the general title *Printed boards and printed board assemblies – Design and use* ¹:

Part 5-1: Attachment (land/joint) considerations – Generic requirements

Part 5-2: Attachment (land/joint) considerations – Discrete components

Part 5-3: Attachment (land/joint) considerations – Gull-wing leads, two sides

Part 5-4: Attachment (land/joint) considerations – J leads, two sides

Part 5-5: Attachment (land/joint) considerations – Gull-wing leads, four sides

Part 5-6: Attachment (land/joint) considerations – Chip carriers with J-leads on four sides

Part 5-7: Attachment (land/joint) considerations – Post (DIP) leads, two sides

The committee has decided that the contents of this publication will remain unchanged until 2004. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

iTeh STANDARD PREVIEW
(standards.iteh.ai)

[SIST EN 61188-5-6:2003](https://standards.iteh.ai/catalog/standards/sist/4eb05737-ac2b-469e-b933-454200a6bbe2/sist-en-61188-5-6-2003)

<https://standards.iteh.ai/catalog/standards/sist/4eb05737-ac2b-469e-b933-454200a6bbe2/sist-en-61188-5-6-2003>

¹ At the time of writing, most of these parts are still to be published.

INTRODUCTION

This part of IEC 61188 covers land patterns for components with J leads on four sides. Each clause contains information in accordance with the following format:

The proposed land pattern dimensions in this standard are based upon the fundamental tolerance calculation combined with the given land protrusions and courtyard excesses (see IEC 61188-5-1). The courtyard covers all issues pertaining to normal manufacturing needs.

The land pattern dimensions covered in this standard are generally applicable for reflowed solder paste processes. For immersion soldering processes (e.g. wave, jet, drag soldering), lands may have to be modified to prevent shadowing and shorting (e.g. by extending land length parallel to the direction of motion of the board and/or provision of solder thieves).

This specification offers a threefold land pattern dimensioning (levels 1, 2, and 3) on the basis of a threefold set of land protrusions and courtyard excesses maximum (max.), median (mdn.), and minimum (min.). Each land pattern has been assigned an identification number to indicate the characteristics of the specific robustness of the land patterns. Users also have the opportunity to organize the information to suit their particular design.

This standard assumes that land dimensions are always larger than component termination or lead outlines. If a user has good reason to use solder resist to limit wetting on a land, or to use lands smaller than component terminations, or to apply a concept different from that of IEC 61188-5-1, this standard may not apply.

It is the responsibility of the user to verify the surface mounting devices (SMD) land patterns used for achieving an undisturbed mounting process, including testing, and an ensured reliability for the product stress conditions when in use.

Dimensions of the components listed in this standard are those available on the market, and are for reference purposes only.