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INTERNATIONAL STANDARD

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Semiconductor devices – Discrete devices –
Part 8: Field-effect transistors

IEC 60747-8:2010-12+AMD1:2021-06 CSV(en)

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SEMICONDUCTOR DEVICES –
DISCRETE DEVICES –

Part 8: Field-effect transistors

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This consolidated version of the official IEC Standard and its amendment has been prepared for user convenience.

IEC 60747-8 edition 3.1 contains the third edition (2010-12) [documents 47E/398/FDIS and 47E/406/RVD] and its amendment 1 (2021-06) [documents 47E/726/CDV and 47E/744/RVC].

In this Redline version, a vertical line in the margin shows where the technical content is modified by amendment 1. Additions are in green text, deletions are in strikethrough red text. A separate Final version with all changes accepted is available in this publication.

International Standard IEC 60747-8 has been prepared by subcommittee 47E: Discrete semiconductor devices, of IEC technical committee 47: Semiconductor devices.

This third edition constitutes a technical revision.

The main changes with respect to the previous edition are listed below.

a) "Clause 3 Classification" was moved and added to Clause 1.
b) "Clause 4 Terminology and letter symbols" was divided into "Clause 3 Terms and definitions" and "Clause 4 Letter symbols" was amended with additions and deletions.
c) Clause 5, 6 and 7 were amended with necessary additions and deletions.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

This Part 8 should be used in conjunction with IEC 60747-1:2006.

A list of all the parts in the IEC 60747 series, under the general title *Semiconductor devices – Discrete devices*, can be found on the IEC website.

Future standards in this series will carry the new general title as cited above. Titles of existing standards in this series will be updated at the time of the next edition.

The committee has decided that the contents of the base publication and its amendment will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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SEMICONDUCTOR DEVICES – DISCRETE DEVICES –

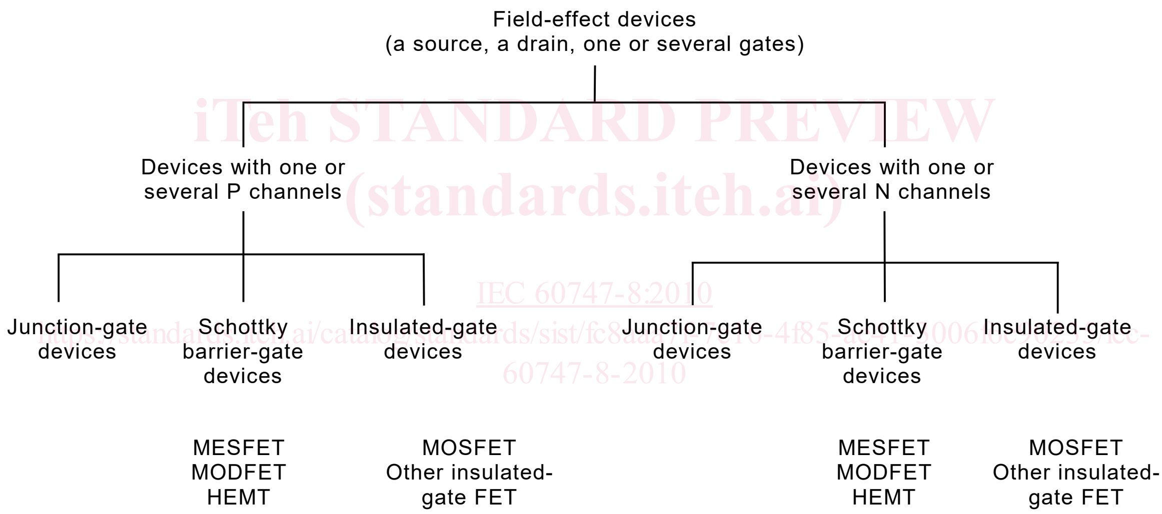
Part 8: Field-effect transistors

1 Scope

This part of IEC 60747 gives standards for the following categories of field-effect transistors:

– type A: junction-gate type;
– type B: insulated-gate depletion (normally on) type;
– type C: insulated-gate enhancement (normally off) type.

Since a field-effect transistor may have one or several gates, the classification shown below results:



NOTE 1 Schottky barrier-gate and insulated gate devices include depletion type devices and enhancement type devices.

NOTE 2 MOSFETs for some applications may not have inverse diode characteristics in the data sheet. Special circuit element structures to eliminate body diode are under development for such applications. MOSFET applications such as motor control equipment need to specify the inverse diode characteristics in the MOSFET to use the inverse diode as a free wheeling diode.

NOTE 3 The graphical symbol only for type C is used in this standard. The standard equally applies for P-channel and for type A and B devices.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61340 (all parts), *Electrostatics*

IEC 60747-1:2006, *Semiconductor devices – Part 1: General*

IEC 60747-7:2000, *Semiconductor devices – Part 7: Bipolar transistors*

IEC 60749-23:2004, *Semiconductor devices – Mechanical and climatic test methods – Part 23: High temperature operating life*

IEC 60749-34, *Semiconductor devices – Mechanical and climatic test methods – Part 34: Power cycling*

3 Terms and definitions

For the purpose of this document, the following terms and definitions apply.

3.1 Types of field-effect transistors

3.1.1
N-channel field-effect transistor
field-effect transistor that has one or more N-type conduction channels

3.1.2
P-channel field-effect transistor
field-effect transistor that has one or more P-type conduction channels

3.1.3
junction-gate field-effect transistor
JFET
field-effect transistor in which

– the source and drain regions are connected with each other by the channel region, all three being of the same conductivity type;

– a gate region adjacent to the channel has the opposite conductivity type, thus forming with source, channel and drain region a PN junction

NOTE The gate-source voltage controls the conductivity of the conduction channel in the channel region by controlling the width of the gate space-charge region and hence also the remaining cross-section of the conduction channel.

3.1.4
insulated-gate field-effect transistor
IGFET
field-effect transistor in which

– one or more gate electrodes are electrically insulated from the body;

– the conductivity type of both the source and drain regions is opposite from that of the semiconductor body in which they are located;

– the principal current flows in a channel that is formed by an inversion layer connecting source and drain regions

NOTE The inversion layer is either already present at zero gate-source voltage or produced within the body at sufficiently high forward gate-source voltage by accumulation of the minority charge carriers of the body material. The conductance of the channel is controlled by the gate-source voltage, which controls the electric field between gate electrode and the body and hence the amount of accumulated minority charge carriers.

3.1.5
metal-oxide-semiconductor field-effect transistor
MOSFET
insulated-gate field-effect transistor in which the insulating layer between each gate electrode and the channel is oxide material

3.1.6
depletion-type (normally on) field-effect transistor
field-effect transistor in which an inversion layer present at the surface of the active semiconductor region causes an appreciable channel conductance that may be increased (decreased) by applying a forward (reverse) gate-source voltage

3.1.7
enhancement-type (normally off) field-effect transistor
field-effect transistor having substantially zero channel conductance at zero gate-source voltage, and in which a conduction channel may be obtained by applying a sufficiently high forward gate-source voltage, which induces an inversion layer below the gate electrode

3.1.8
single-gate field-effect transistor
field-effect transistor having a gate region, a source region, and a drain region

NOTE The term may be abbreviated to "field-effect transistor", if no ambiguity is likely to occur.

3.1.9
dual-gate field-effect transistor
field-effect transistor having two independent gate regions, a source region, and a drain region

3.1.10
schottky-barrier-gate field-effect transistor
field-effect transistor in which

– the source and drain regions are connected with each other by the channel region, all three being of the same conductivity type;
– one or more gate electrodes each form a Schottky-barrier with the channel region;

the gate-source voltage controls the conductance of the conduction channel by varying its cross-section

3.1.11
metal-semiconductor field-effect transistor
MESFET
Schottky-barrier-gate field-effect transistor in which the gate electrodes are metal

3.1.12
modulation-doped field-effect transistor or high electron mobility transistor
MODFET or HEMT
metal-semiconductor field-effect transistor in which a doped material forms a heterojunction with an undoped channel; the doped material supplies electrons to the undoped channel whose high electron mobility results in enhanced channel conductance

NOTE MODFET and HEMT should be used interchangeably.

3.2 General terms

3.2.1 Physical regions (of a field-effect transistor)

3.2.1.1
source (of a field-effect transistor)
physical region that is designed by the manufacturer to contain the supply region under the defined operating conditions to which the specifications refer

3.2.1.2
drain (of a field-effect transistor)
physical region that is designed by the manufacturer to contain the collection region under the defined operating conditions to which the specifications refer

3.2.1.3
gate (of an IGFET)
insulating layer between the gate electrode and the surface of the semiconductor body, below which the channel is or may be formed

3.2.1.4
gate (of an JFET)
region below the gate electrode that is of opposite conductivity type from that of the source, channel and drain regions

3.2.1.5
channel (of a depletion-type IGFET)
inversion layer technologically placed below the gate region

3.2.1.6
channel (of a JFET)
region between source region and drain region that has the same conductivity type as these two regions

3.2.1.7
subchannel (of an IGFET)
region between source region and drain region, excluding the channel region of a depletion-type IGFET and all pertinent transition zones

3.2.1.8
substrate (of a JFET or IGFET)
part of the original material that remains unchanged when the device elements are formed upon or within the original material

NOTE The original material may be a layer of semiconductor material cut from a single crystal, a layer of semiconductor material deposited on a supporting base, or the supporting base itself.

3.2.1.9
substrate (of a JFET or IGFET)
original semiconductor material before being processed

NOTE The intended meaning will become clear from the context in which the term is used. If necessary, distinction could be made between the "original substrate" and the "remaining substrate".

3.2.1.10
substrate (of a thin-film field-effect transistor)
insulator that supports the source and drain electrodes, the insulating gate layer, and the thin semiconductor layer

3.2.2 Functional regions

3.2.2.1
functional source region
supply region that delivers principal-current charge carriers into the channel

3.2.2.2
functional drain region
collection region that acquires principal-current charge carriers from the channel