

INTERNATIONAL STANDARD

NORME INTERNATIONALE

**Semiconductor devices – Discrete devices –
Part 8: Field-effect transistors**

(standards.iteh.ai)

**Dispositifs à semiconducteurs – Dispositifs discrets –
Partie 8: Transistors à effet de champ**

IEC 60747-8:2010
<https://standards.iteh.ai/catalog/standards/sist/fc8aaa7f-7c16-4f85-ae41-3006f6c90235/iec-60747-8-2010>



THIS PUBLICATION IS COPYRIGHT PROTECTED
Copyright © 2010 IEC, Geneva, Switzerland

All rights reserved. Unless otherwise specified, no part of this publication may be reproduced or utilized in any form or by any means, electronic or mechanical, including photocopying and microfilm, without permission in writing from either IEC or IEC's member National Committee in the country of the requester.

If you have any questions about IEC copyright or have an enquiry about obtaining additional rights to this publication, please contact the address below or your local IEC member National Committee for further information.

Droits de reproduction réservés. Sauf indication contraire, aucune partie de cette publication ne peut être reproduite ni utilisée sous quelque forme que ce soit et par aucun procédé, électronique ou mécanique, y compris la photocopie et les microfilms, sans l'accord écrit de la CEI ou du Comité national de la CEI du pays du demandeur.

Si vous avez des questions sur le copyright de la CEI ou si vous désirez obtenir des droits supplémentaires sur cette publication, utilisez les coordonnées ci-après ou contactez le Comité national de la CEI de votre pays de résidence.

IEC Central Office
3, rue de Varembe
CH-1211 Geneva 20
Switzerland
Email: inmail@iec.ch
Web: www.iec.ch

About the IEC

The International Electrotechnical Commission (IEC) is the leading global organization that prepares and publishes International Standards for all electrical, electronic and related technologies.

About IEC publications

The technical content of IEC publications is kept under constant review by the IEC. Please make sure that you have the latest edition, a corrigenda or an amendment might have been published.

- Catalogue of IEC publications: www.iec.ch/searchpub

The IEC on-line Catalogue enables you to search by a variety of criteria (reference number, text, technical committee,...). It also gives information on projects, withdrawn and replaced publications.

- IEC Just Published: www.iec.ch/online_news/justpub

Stay up to date on all new IEC publications. Just Published details twice a month all new publications released. Available on-line and also by email.

- Electropedia: www.electropedia.org

The world's leading online dictionary of electronic and electrical terms containing more than 20 000 terms and definitions in English and French, with equivalent terms in additional languages. Also known as the International Electrotechnical Vocabulary online.

- Customer Service Centre: www.iec.ch/webstore/custserv

If you wish to give us your feedback on this publication or need further assistance, please visit the Customer Service Centre FAQ or contact us:

Email: csc@iec.ch

Tel.: +41 22 919 02 11

Fax: +41 22 919 03 00

A propos de la CEI

La Commission Electrotechnique Internationale (CEI) est la première organisation mondiale qui élabore et publie des normes internationales pour tout ce qui a trait à l'électricité, à l'électronique et aux technologies apparentées.

A propos des publications CEI

Le contenu technique des publications de la CEI est constamment revu. Veuillez vous assurer que vous possédez l'édition la plus récente, un corrigendum ou amendement peut avoir été publié.

- Catalogue des publications de la CEI: www.iec.ch/searchpub/cur_fut-f.htm

Le Catalogue en-ligne de la CEI vous permet d'effectuer des recherches en utilisant différents critères (numéro de référence, texte, comité d'études,...). Il donne aussi des informations sur les projets et les publications retirées ou remplacées.

- Just Published CEI: www.iec.ch/online_news/justpub

Restez informé sur les nouvelles publications de la CEI. Just Published détaille deux fois par mois les nouvelles publications parues. Disponible en-ligne et aussi par email.

- Electropedia: www.electropedia.org

Le premier dictionnaire en ligne au monde de termes électroniques et électriques. Il contient plus de 20 000 termes et définitions en anglais et en français, ainsi que les termes équivalents dans les langues additionnelles. Egalement appelé Vocabulaire Electrotechnique International en ligne.

- Service Clients: www.iec.ch/webstore/custserv/custserv_entry-f.htm

Si vous désirez nous donner des commentaires sur cette publication ou si vous avez des questions, visitez le FAQ du Service clients ou contactez-nous:

Email: csc@iec.ch

Tél.: +41 22 919 02 11

Fax: +41 22 919 03 00



IEC 60747-8

Edition 3.0 2010-12

INTERNATIONAL STANDARD

NORME INTERNATIONALE

**Semiconductor devices – Discrete devices –
Part 8: Field-effect transistors**

**Dispositifs à semiconducteurs – Dispositifs discrets –
Partie 8: Transistors à effet de champ**

INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

COMMISSION
ELECTROTECHNIQUE
INTERNATIONALE

ICS 31.080.30

PRICE CODE
CODE PRIX

XC

ISBN 978-2-88912-279-0

CONTENTS

FOREWORD.....	6
1 Scope.....	8
2 Normative references.....	8
3 Terms and definitions.....	9
3.1 Types of field-effect transistors.....	9
3.2 General terms.....	10
3.2.1 Physical regions (of a field-effect transistor).....	10
3.2.2 Functional regions.....	11
3.3 Terms related to ratings and characteristics.....	12
3.4 Conventional used terms	17
4 Letter symbols.....	17
4.1 General.....	17
4.2 Additional general subscripts.....	17
4.3 List of letter symbols	17
4.3.1 Voltage	17
4.3.2 Currents.....	18
4.3.3 Power dissipation.....	18
4.3.4 Small-signal parameters	18
4.3.5 Other parameters.....	20
4.3.6 Matched-pair field-effect transistors.....	21
4.3.7 Inverse diodes integrated in MOSFETs.....	21
5 Essential ratings and characteristics.....	22
5.1 General.....	22
5.1.1 Device categories.....	22
5.1.2 Multiple-gate devices.....	22
5.1.3 Handling precautions.....	22
5.2 Ratings (limiting values).....	22
5.2.1 Temperatures	22
5.2.2 Power dissipation (P_{tot}).....	22
5.2.3 Safe operating area (SOA) for MOSFET only.....	22
5.2.4 Voltages and currents.....	23
5.3 Characteristics.....	23
5.3.1 Characteristics for low-frequency amplifier.....	23
5.3.2 Characteristics for high-frequency amplifier	25
5.3.3 Characteristics for high and low power switching and chopper	27
5.3.4 Characteristics for low-level amplifier	30
5.3.5 Characteristics for voltage-controlled resistor.....	32
5.3.6 Specific characteristics of matched-pair field-effect transistors for low-frequency differential	33
6 Measuring methods	34
6.1 General.....	34
6.2 Verification of ratings (limiting values).....	34
6.2.1 Voltages and currents.....	34
6.2.2 Safe operating area.....	40
6.2.3 Avalanche energy	44
6.3 Methods of measurement.....	46

6.3.1	Breakdown voltage, drain to source ($V_{(BR)DS^*}$)	46
6.3.2	Gate-source off-state voltage ($V_{GS(off)}$) (type A and B), gate source threshold voltage ($V_{GS(th)}$) (type C)	47
6.3.3	Drain leakage current (d.c.) (I_{DS^*})(type C), Drain cut-off current (d.c.) (I_{DSX}) (type A and B)	48
6.3.4	Gate cut-off current (I_{GS^*})(type A), Gate-leakage current (I_{GS^*})(type B and C)	48
6.3.5	(Static) drain-source on-state resistance ($r_{DS(on)}$) or drain-source on-state voltage ($V_{DS(on)}$)	49
6.3.6	Switching times ($t_{d(on)}$, t_r , $t_{d(off)}$, and t_f)	51
6.3.7	Turn-on power dissipation (P_{on}), turn-on energy (per pulse) (E_{on})	52
6.3.8	Turn-off power dissipation (P_{off}), turn-off energy (per pulse) (E_{off})	53
6.3.9	Gate charges (Q_G , Q_{GD} , $Q_{GS(th)}$, $Q_{GS(pl)}$)	53
6.3.10	Common source short-circuit input capacitance (C_{iss})	54
6.3.11	Common source short-circuit output capacitance (C_{oss})	55
6.3.12	Common source short-circuit reverse transfer capacitance (C_{rss})	56
6.3.13	Internal gate resistance (r_g)	57
6.3.14	MOSFET forward recovery time (t_{fr}) and MOSFET forward recovered charge (Q_f)	58
6.3.15	Drain-source reverse voltage (V_{DSR})	62
6.3.16	Small-signal short-circuit output conductance (type A, B and C) (g_{oss})	62
6.3.17	Small-signal short-circuit forward transconductance (types A, B and C)	65
6.3.18	Noise (types A, B and C) (F , V_n)	67
6.3.19	On-state drain-source resistance (under small-signal conditions) ($r_{ds(on)}$)	68
6.3.20	Channel-case transient thermal impedance ($Z_{th(j-c)}$) and thermal resistance ($R_{th(j-c)}$) of a field-effect transistor	69
7	Acceptance and reliability	71
7.1	General requirements	71
7.2	Acceptance-defining characteristics	71
7.3	Endurance and reliability tests	72
7.3.1	High-temperature blocking (HTRB)	72
7.3.2	High-temperature gate bias	72
7.3.3	Intermittent operating life (load cycles)	72
7.4	Type tests and routine tests	73
7.4.1	Type tests	73
7.4.2	Routine tests	73
	Bibliography	75
	Figure 1 – Basic waveforms to specify the gate charges	14
	Figure 2 – Integral times for the turn-on energy E_{on} and turn-off energy E_{off}	16
	Figure 3 – Switching times	21
	Figure 4 – Circuit diagram for testing of drain-source voltage	35
	Figure 5 – Circuit diagram for testing of gate-source voltage	35
	Figure 6 – Circuit diagram for testing of gate-drain voltage	36
	Figure 7 – Basic circuit for the testing of drain current	37
	Figure 8 – Circuit diagram for testing of peak drain current	38
	Figure 9 – Basic circuit for the testing of reverse drain current of MOSFETs	38

Figure 10 – Basic circuit for the testing of peak reverse drain current of MOSFETs	39
Figure 11 – Circuit diagram for verifying FBSOA	40
Figure 12 – Circuit diagram for verifying RBSOA.....	41
Figure 13 – Test waveforms for verifying RBSOA.....	41
Figure 14 – Circuit for testing safe operating pulse duration at load short circuit	42
Figure 15 – Waveforms of gate-source voltage V_{GS} , drain current I_D and voltage V_{DS} during load short circuit condition SCSOA.....	43
Figure 16 – Circuit for the inductive avalanche switching	44
Figure 17 – Waveforms of I_D , V_{DS} and V_{GS} during unclamped inductive switching.....	44
Figure 18 – Waveforms of I_D , V_{DS} and V_{GS} for the non-repetitive avalanche switching	45
Figure 19 – Circuit diagrams for the measurement drain-source breakdown voltage	46
Figure 20 – Circuit diagram for measurement of gate-source off-state voltage and gate-source threshold voltage	47
Figure 21 – Circuit diagram for drain leakage (or off-state) current or drain cut-off current measurement.....	48
Figure 22 – Circuit diagram for measuring of gate cut-off current or gate leakage current	49
Figure 23 – Basic circuit of measurement for on-state resistance	50
Figure 24 – On-state resistance	50
Figure 25 – Circuit diagram for switching time	51
Figure 26 – Schematic switching waveforms and times.....	51
Figure 27 – Circuit for determining the turn-on and turn-off power dissipation and/or energy.....	52
Figure 28 – Circuit diagrams for the measurement gate charges.....	54
Figure 29 – Basic for the measurement of short-circuit input capacitance	55
Figure 30 – Basic circuit for measurement of short-circuit output capacitance (C_{OSS}).....	56
Figure 31 – Circuit for measurement of reverse transfer capacitance C_{rss}	57
Figure 32 – Circuit for measurement of internal gate resistance	58
Figure 33 – Circuit diagram for MOSFET forward recovery time and recovered charge (Method 1).....	59
Figure 34 – Current waveform through MOSFET (Method 1)	59
Figure 35 – Circuit diagram for MOSFET forward recovery time and recovered charge (Method 2).....	60
Figure 36 – Current waveform through MOSFET (Method 2)	61
Figure 37 – Circuit diagram for the measurement of drain-source reverse voltage	62
Figure 38 – Basic circuit for the measurement of the output conductance g_{OSS} (method 1: null method).....	63
Figure 39 – Basic circuit for the measurement of the output conductance g_{OSS} (method 2: two-voltmeter method)	64
Figure 40 – Circuit for the measurement of short-circuit forward transconductance g_{fs} (Method 1: Null method).....	65
Figure 41 – Circuit for the measurement of forward transconductance g_{fs} (method 2: two-voltmeter method)	66
Figure 42 – Block diagram for the measurement of equivalent input noise voltage.....	67
Figure 43 – Circuit for the measurement of equivalent input noise voltage.....	67
Figure 44 – Circuit diagram for the measurement of on-state drain-source resistance.....	68

Figure 45 – Circuit diagram	69
Figure 46 – Circuit for high-temperature blockings	72
Figure 47 – Circuit for high-temperature gate bias.....	72
Figure 48 – Circuit for intermittent operating life	73
Table 1 – Terms for MOSFET in this standard and the conventional used terms for the inverse diode integrated in the MOSFET	17
Table 2 – Acceptance defining characteristics	34
Table 3 – Acceptance-defining characteristics for endurance and reliability tests	71
Table 4 – Minimum type and routine tests for FETs when applicable.....	74

iTeh STANDARD PREVIEW **(standards.iteh.ai)**

IEC 60747-8:2010

<https://standards.iteh.ai/catalog/standards/sist/fc8aaa7f-7c16-4f85-ae41-3006f6c90235/iec-60747-8-2010>

INTERNATIONAL ELECTROTECHNICAL COMMISSION

**SEMICONDUCTOR DEVICES –
DISCRETE DEVICES –****Part 8: Field-effect transistors****FOREWORD**

- 1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
- 2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
- 3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
- 4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
- 5) IEC itself does not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC is not responsible for any services carried out by independent certification bodies.
- 6) All users should ensure that they have the latest edition of this publication.
- 7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
- 8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
- 9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 60747-8 has been prepared by subcommittee 47E: Discrete semiconductor devices, of IEC technical committee 47: Semiconductor devices.

This third edition of IEC 60747-8 cancels and replaces the second edition published in 2000. This third edition constitutes a technical revision.

The main changes with respect to the previous edition are listed below.

- a) "Clause 3 Classification" was moved and added to Clause 1.
- b) "Clause 4 Terminology and letter symbols" was divided into "Clause 3 Terms and definitions" and "Clause 4 Letter symbols" was amended with additions and deletions.
- c) Clause 5, 6 and 7 were amended with necessary additions and deletions.

The text of this standard is based on the following documents:

FDIS	Report on voting
47E/398/FDIS	47E/406/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

This Part 8 should be used in conjunction with IEC 60747-1:2006.

A list of all the parts in the IEC 60747 series, under the general title *Semiconductor devices – Discrete devices*, can be found on the IEC website.

Future standards in this series will carry the new general title as cited above. Titles of existing standards in this series will be updated at the time of the next edition.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "<http://webstore.iec.ch>" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

iTeh STANDARD PREVIEW
(standards.iteh.ai)

IEC 60747-8:2010

<https://standards.iteh.ai/catalog/standards/sist/fc8aaa7f-7c16-4f85-ae41-3006f6c90235/iec-60747-8-2010>

SEMICONDUCTOR DEVICES – DISCRETE DEVICES –

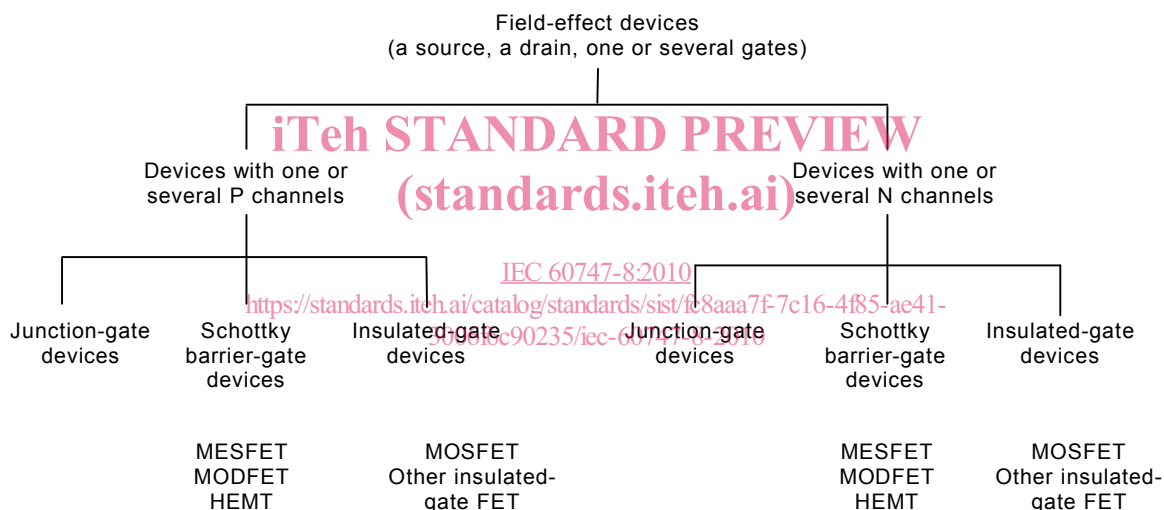
Part 8: Field-effect transistors

1 Scope

This part of IEC 60747 gives standards for the following categories of field-effect transistors:

- type A: junction-gate type;
- type B: insulated-gate depletion (normally on) type;
- type C: insulated-gate enhancement (normally off) type.

Since a field-effect transistor may have one or several gates, the classification shown below results:



NOTE 1 Schottky barrier-gate and insulated gate devices include depletion type devices and enhancement type devices.

NOTE 2 MOSFETs for some applications may not have inverse diode characteristics in the data sheet. Special circuit element structures to eliminate body diode are under development for such applications. MOSFET applications such as motor control equipment need to specify the inverse diode characteristics in the MOSFET to use the inverse diode as a free wheeling diode.

NOTE 3 The graphical symbol only for type C is used in this standard. The standard equally applies for P-channel and for type A and B devices.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61340 (all parts), *Electrostatics*

IEC 60747-1:2006, *Semiconductor devices – Part 1: General*

IEC 60747-7:2000, *Semiconductor devices – Part 7: Bipolar transistors*

IEC 60749-23:2004, *Semiconductor devices – Mechanical and climatic test methods – Part 23: High temperature operating life*

IEC 60749-34, *Semiconductor devices – Mechanical and climatic test methods – Part 34: Power cycling*

3 Terms and definitions

For the purpose of this document, the following terms and definitions apply.

3.1 Types of field-effect transistors

3.1.1

N-channel field-effect transistor

field-effect transistor that has one or more N-type conduction channels

3.1.2

P-channel field-effect transistor

field-effect transistor that has one or more P-type conduction channels

3.1.3

junction-gate field-effect transistor

JFET

field-effect transistor in which

- the source and drain regions are connected with each other by the channel region, all three being of the same conductivity type;
- a gate region adjacent to the channel has the opposite conductivity type, thus forming with source, channel and drain region a PN junction

NOTE The gate-source voltage controls the conductivity of the conduction channel in the channel region by controlling the width of the gate space-charge region and hence also the remaining cross-section of the conduction channel.

3.1.4

insulated-gate field-effect transistor

IGFET

field-effect transistor in which

- one or more gate electrodes are electrically insulated from the body;
- the conductivity type of both the source and drain regions is opposite from that of the semiconductor body in which they are located;
- the principal current flows in a channel that is formed by an inversion layer connecting source and drain regions

NOTE The inversion layer is either already present at zero gate-source voltage or produced within the body at sufficiently high forward gate-source voltage by accumulation of the minority charge carriers of the body material. The conductance of the channel is controlled by the gate-source voltage, which controls the electric field between gate electrode and the body and hence the amount of accumulated minority charge carriers.

3.1.5

metal-oxide-semiconductor field-effect transistor

MOSFET

insulated-gate field-effect transistor in which the insulating layer between each gate electrode and the channel is oxide material

3.1.6

depletion-type (normally on) field-effect transistor

field-effect transistor in which an inversion layer present at the surface of the active semiconductor region causes an appreciable channel conductance that may be increased (decreased) by applying a forward (reverse) gate-source voltage

3.1.7

enhancement-type (normally off) field-effect transistor

field-effect transistor having substantially zero channel conductance at zero gate-source voltage, and in which a conduction channel may be obtained by applying a sufficiently high forward gate-source voltage, which induces an inversion layer below the gate electrode

3.1.8

single-gate field-effect transistor

field-effect transistor having a gate region, a source region, and a drain region

NOTE The term may be abbreviated to "field-effect transistor", if no ambiguity is likely to occur.

3.1.9

dual-gate field-effect transistor

field-effect transistor having two independent gate regions, a source region, and a drain region

3.1.10

schottky-barrier-gate field-effect transistor

field-effect transistor in which

- the source and drain regions are connected with each other by the channel region, all three being of the same conductivity type;
- one or more gate electrodes each form a Schottky-barrier with the channel region;

the gate-source voltage controls the conductance of the conduction channel by varying its cross-section

3.1.11

metal-semiconductor field-effect transistor

MESFET

Schottky-barrier-gate field-effect transistor in which the gate electrodes are metal

3.1.12

modulation-doped field-effect transistor or high electron mobility transistor MODFET or HEMT

metal-semiconductor field-effect transistor in which a doped material forms a heterojunction with an undoped channel; the doped material supplies electrons to the undoped channel whose high electron mobility results in enhanced channel conductance

NOTE MODFET and HEMT should be used interchangeably.

3.2 General terms

3.2.1 Physical regions (of a field-effect transistor)

3.2.1.1

source (of a field-effect transistor)

physical region that is designed by the manufacturer to contain the supply region under the defined operating conditions to which the specifications refer

3.2.1.2**drain (of a field-effect transistor)**

physical region that is designed by the manufacturer to contain the collection region under the defined operating conditions to which the specifications refer

3.2.1.3**gate (of an IGFET)**

insulating layer between the gate electrode and the surface of the semiconductor body, below which the channel is or may be formed

3.2.1.4**gate (of an JFET)**

region below the gate electrode that is of opposite conductivity type from that of the source, channel and drain regions

3.2.1.5**channel (of a depletion-type IGFET)**

inversion layer technologically placed below the gate region

3.2.1.6**channel (of a JFET)**

region between source region and drain region that has the same conductivity type as these two regions

3.2.1.7**subchannel (of an IGFET)**

region between source region and drain region, excluding the channel region of a depletion-type IGFET and all pertinent transition zones

3.2.1.8**substrate (of a JFET or IGFET)**

part of the original material that remains unchanged when the device elements are formed upon or within the original material

NOTE The original material may be a layer of semiconductor material cut from a single crystal, a layer of semiconductor material deposited on a supporting base, or the supporting base itself.

3.2.1.9**substrate (of a JFET or IGFET)**

original semiconductor material before being processed

NOTE The intended meaning will become clear from the context in which the term is used. If necessary, distinction could be made between the "original substrate" and the "remaining substrate".

3.2.1.10**substrate (of a thin-film field-effect transistor)**

insulator that supports the source and drain electrodes, the insulating gate layer, and the thin semiconductor layer

3.2.2 Functional regions**3.2.2.1****functional source region**

supply region that delivers principal-current charge carriers into the channel

3.2.2.2**functional drain region**

collection region that acquires principal-current charge carriers from the channel

3.2.2.3

channel (of a IGFET)

functional region through which the principal-current charge carriers pass and in which the carrier concentration is determined by the gate-source voltage, the principal current being the result of the drift field produced by the drain-source voltage

3.2.2.4

channel (of a JFET)

functional region through which the principal-current charge carriers pass and whose cross-section is determined by the applied gate-source voltage, the principal current being the result of the drift field produced by the drain-source voltage

3.2.2.5

subchannel space-charge region (of an IGFET)

space-charge region associated with the transition regions between the subchannel region on one side, and source region, channel region and drain region on the other side

3.2.2.6

functional subchannel region

remaining neutral part of the (physical) subchannel region that is confined by the surrounding subchannel space-charge region

3.3 Terms related to ratings and characteristics

3.3.1

gate cut-off current (of a junction-gate field-effect transistor)

current flowing in the gate terminal of a junction field-effect transistor when the pn junction is biased in the reverse direction

3.3.2

gate leakage current (of an insulated-gate field-effect transistor)

leakage current through the insulated-gate of an insulated-gate field-effect transistor

3.3.3

capacitances

3.3.3.1

(short-circuit) input capacitance

capacitance between the gate and source terminals with the drain terminal short-circuited to the source terminal for a.c. signals

3.3.3.2

(short-circuit) output capacitance

capacitance between the drain and source terminals with the gate terminal short-circuited to the source terminal for a.c. signals

3.3.3.3

reverse transfer capacitance

capacitance between the drain and gate terminals excluding parallel capacitances between drain and source, and gate and source

3.3.4

gate-source resistance

d.c. resistance between gate and source terminals at specified gate-source and drain-source voltages

3.3.5

drain-source on-state resistance

d.c. resistance between the drain and source terminals when the FET is in its on-state

3.3.6**gate charge**

charge required to raise the gate-source voltage from zero to a specified value

3.3.6.1**total gate charge**

charge that is required to raise the gate-source voltage from zero to a specified value and calculated by the equation below (see Figure 1)

$$Q_G = \int_{t_0}^{t_4} i_{GG}(t) dt$$

3.3.6.2**threshold gate charge**

charge required to raise gate-source from zero to $V_{GS(th)}$ and calculated by the equation below (see Figure 1)

$$Q_{GS(th)} = \int_{t_0}^{t_1} i_{GG}(t) dt$$

3.3.6.3**plateau gate charge**

charge required to raise gate-source voltage from zero to plateau voltage $V_{GS(pl)}$ and calculated by the equation below (see Figure 1)

$$Q_{GS(pl)} = \int_{t_0}^{t_2} i_{GG}(t) dt$$

3.3.6.4**gate drain charge**

charge difference between beginning and end of plateau region, required to charge up C_{GD} and calculated by the equation below (see Figure 1)

$$Q_{GD} = \int_{t_2}^{t_3} i_{GG}(t) dt$$

ITih STANDARD PREVIEW
(standards.iteh.ai)

[IEC 60747-8:2010](https://standards.iteh.ai/catalog/standards/sist/fc8aaa7f-7c16-4f85-ae41-3006f6c90235/iec-60747-8-2010)

<https://standards.iteh.ai/catalog/standards/sist/fc8aaa7f-7c16-4f85-ae41-3006f6c90235/iec-60747-8-2010>