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Delay and power calculation standards –

Part 3: Standard Delay Format (SDF) for the electronic design process

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DELAY AND POWER CALCULATION STANDARDS –

Part 3: Standard Delay Format (SDF) for the electronic design process

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The text of this standard is based on the following documents:

IEEE Std	FDIS	Report on voting
1497 (2001)	93/191/FDIS	93/196/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives.

The committee has decided that the contents of this publication will remain unchanged until 2006.

IEC 61523 consists of the following parts, under the general title *Delay and power calculation standards*:

IEC 61523-1, Part 1: *Integrated circuit delay and power calculation systems*

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IEC 61523-2, Part 2: *Pre-layout delay calculation specification of CMOS ASIC libraries*

IEC/IEEE 61523-3, Part 3: *Standard Delay Format (SDF) for the electronic process*

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IEEE Standard for Standard Delay Format (SDF) for the Electronic Design Process

Sponsor

Design Automation Standards Committee of the IEEE Computer Society

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Approved 5 December 2001

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Abstract: The Standard Delay Format (SDF) is defined in this standard. SDF is a textual file format for representing the delay and timing information of electronic systems. While both human and machine readable, in its most common usage it will be machine written and machine read in support of timing analysis and verification tools, and of other tools requiring delay and timing information. The primary audience for this standard is the implementors of tools supporting the format, but anyone with a need to understand the format's contents will find it useful.

Keywords: computer, computer languages, delay, delay backannotation, digital systems, electronic systems, hardware, hardware design, SDF, timing, timing analysis, timing backannotation, timing verification

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IEEE Introduction

The Standard Delay Format (SDF) was designed to serve as a simple textual medium for communicating timing information and constraints between EDA tools. The original version was designed by Rajit C. Chandra in 1990 while at Cadence Design Systems, and was intended as a means of communicating macrocell and interconnect delays from Gate Ensemble to Verilog-XL, Veritime and other stand-alone tools requiring timing data.

Because it was originally targeted for annotation to tools using the Verilog language, many SDF constructs are analogous to those in Verilog specify blocks. Those already familiar with the Verilog specify block will find many of the SDF constructs familiar, such as SETUP and PATHPULSE. SDF also includes constructs for annotating interconnect delays, and can be used for forward annotation by specifying path delay constraints from timing analysis to floorplanners, and synthesis and layout tools.

SDF was first introduced into the EDA marketplace in 1991 where it won quick acceptance. Cadence placed SDF in the public domain in 1992 when it turned control over to Open Verilog International (OVI), and OVI delivered the first SDF standard, version 2.0, in June, 1993 (SDF version 1.0 was used by Cadence). OVI has since introduced version 2.1 in February, 1994, and version 3.0 in May, 1995. VHDL (IEEE 1076) also takes advantage of SDF through the VITAL standard.

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In 1996 the OVI Board of Directors began an effort to establish SDF as an IEEE standard. With the approval of the IEEE Design Automation Standards Committee (DASC), the OVI Logic Modeling Technical Subcommittee became the IEEE SDF Study Group. With the approval of the Project Authorization Request (PAR) by the IEEE Standards Board on February 10, 1997, this group became the IEEE SDF Working Group.

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This IEEE SDF standard builds upon OVI SDF version 3.0, and will be known as version 4.0. The changes from OVI 3.0 to IEEE 4.0 are small (LABEL construct added, NETDELAY construct restored), but the change from OVI standard to IEEE standard is significant, and so this is recognized by a new version number.

Objective

The starting point for the IEEE P1497 SDF Working Group was the OVI LRM version 3.0 SDF standard, with the goal of soliciting further enhancements and improving the quality and rigor of the LRM. Since SDF is already in widespread use, no modifications that would invalidate current usage were considered.

Acknowledgments

This standard is based on work originally developed by Cadence Design Systems, Inc. (in SDF 1.0) and Open Verilog International (in SDF 2.0, 2.1 and 3.0). The IEEE is grateful to Cadence Design Systems and Open Verilog International for permission to use their materials as the basis for this standard.

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DELAY AND POWER CALCULATION STANDARDS –
Part 3: Standard Delay Format (SDF)
for the electronic design process

1. Overview

1.1 Scope

The Standard Delay Format (SDF) is an existing OVI standard for the representation and interpretation of timing data for use at any stage of the electronic design process. The ASCII data in the SDF file is represented in a tool and language independent way and includes path delays, timing constraint values, interconnect delays and high level technology parameters. This standard describes the IEEE version of the SDF standard.

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This standard should serve as a complete specification of the Standard Delay Format (SDF). It contains:

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- Detailed information on how SDF is used in the design process.
- Detailed semantic descriptions of all SDF constructs.
- The formal syntax.
- Examples.

1.2 Organization of this standard

A synopsis of the clauses and annexes of this standard is presented as a quick reference. There are five clauses and two annexes. All the clauses and annexes are normative parts of this standard, with the exception of Annex B (informative).

Clause 1: Overview—Content overview.

Clause 2: References—References to other applicable standards that are assumed or required for SDF.

Clause 3: Definitions and conventions—Introduction to syntactic style and the major syntactic components.

Clause 4: SDF in the design process—The role and use of SDF in the design process.

Clause 5: Defining the Standard Delay Format—The content of an SDF file. For each part of the file, the purpose is discussed, the syntax is specified, the semantics are explained, and examples are presented.

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Annex A: Syntax of SDF—SDF file syntax description. The syntax of the contents of an SDF file is described in this annex.

Annex B: SDF file examples—Informative examples of SDF files.

2. References

This standard shall be used in conjunction with the following publications. When the following standards are superseded by an approved revision, the revision shall apply.

IEEE Std 1076, 2000 Edition, IEEE Standard VHDL Language Reference Manual.[1]

IEEE Std 1364-2001, IEEE Standard Verilog® Hardware Description Language.

3. Conventions

3.1 Terminology conventions

The verb “shall” is used throughout this standard to indicate mandatory requirements, whereas the verb “can” is used to indicate optional features that can be used at discretion. If “can” is used, however, one must follow the requirements set forth by the format definition. The verb “shall” denotes different meanings to different readers of this standard:

a) To the developers of tools that process SDF, the verb “shall” denotes a requirement that the standard imposes. The resulting implementation is required to enforce the requirements and to issue an error if the requirement is not met by the input.

b) To the human reader of SDF, the verb “shall” denotes that those characteristics of SDF are natural consequences of the format definition. The characteristics thereby implied in the SDF source text can be depended upon.

c) To the developer of tools that write SDF, and to the human writer of SDF, the verb “shall” denotes that those characteristics of SDF are natural consequences of the format definition. Adherence to the constraint implied by the characteristic is required.

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3.2 Syntactic conventions

3.2.1 Syntactic conventions

The formal syntax of SDF is described using Backus-Naur Form (BNF). In addition, the following conventions are used:

a) Lowercase italic words, some containing embedded underscores, are used to denote syntactic tokens. For example:

   module_declaration

b) Boldface words are used to denote reserved keywords, operators, and punctuation marks as a required part of the syntax. For example:

   IOPATH
   (
)

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c) A vertical bar separates alternative items unless it appears in boldface, in which case it stands for itself. In most cases each alternative appears on a separate line. For example:

character ::=
alphanumeric
/escaped_character

When the alternatives are very simple, as in the case of single characters, then they can appear on a single line or on consecutive multiple lines. For example:

decimal_digit ::= ***0*** */* ***1*** */* ***2*** */* ***3*** */* ***4*** */* ***5*** */* ***6*** */* *7* */* ***8*** */* ***9***

d) Square brackets enclose optional items. For example:

real_number ::= integer [**.** *integer]*

e) Braces enclose a repeated item unless it appears in boldface, in which case it stands for itself. The item can appear zero or more times; the repetitions occur from left to right as with an equivalent left-recursive rule. Thus, this rules says that a CELL can contain any number of timing specifications:

cell ::= **(** ***CELL*** *celltype cell_instance { timing_spec }* **)**

`A constant-width` font is used for examples, file names, and while referring to constants, especially `0`, `1`, `x`, and `z` values.

3.2.2 Lexical tokens

An SDF file is a stream of lexical tokens in free format, each of which consists of one or more characters. Spaces and newlines serve only to separate tokens.

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3.2.3 White space

Tabs, spaces, and newlines are considered white space. White space is never significant except when used within quoted strings or to separate lexical tokens.

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3.2.4 Comments

Comments can be placed in SDF files using either the “C” or “C++” style.

“C”-style comments begin with /* and end with */. Nesting of “C”-style comments is not permitted. “C”-style comments can appear anywhere except within lexical tokens or quoted strings.

“C++”-style comments begin with // and continue until the end of the current line (the next newline character). Annotators shall ignore the double-slash and any text after them on any line in the file.

3.2.5 Identifiers

Identifiers can consist of alphanumeric characters and special characters. Alphanumeric characters consist of the letters of the alphabet, the numeric base-10 digits, the underscore (‘_’), and the dollar sign (‘$’). Special characters must be escaped (preceded with the backslash (‘\’) character) in order to be used in an identifier. The special characters are:

! " # $ % & « ( ) * + , - . / : ; < = > ? @ [\ ] ^ ‘ { | } ~

Any character can be escaped with a backslash, and the backslash is only required for special characters. Note that if a character normally has any special meaning in an identifier, this is lost when the character is escaped.

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3.2.6 Quoted strings

A quoted string is a string of any legal SDF characters, including white space, that are enclosed between double-quotes (‘"’). Except for the double-quote itself, special characters lose their special meaning in a quoted string. The double-quote character may be included in a quoted string by escaping it [preceding it with the backslash (‘\’) character].

3.2.7 Bit specifications

A bit specification is indicated by an identifier with trailing paired square brackets (‘**[**’ and ‘**]**’). A single bit is indicated by a single integer between the square brackets, while a bit range is indicated by two integers separated by a colon (‘**:**’).

3.2.8 Hierarchy divider character

Either the period (‘**.**’) or the slash (‘**/**’) can be established as the hierarchy divider character, as described in 5.2.7. This character only has this special meaning when used to separate identifiers. An escaped hierarchy divider character loses its meaning as a hierarchy divider.

3.2.9 Data values

A number shall be an integer or a real number. Real numbers can be expressed in scientific notation, and can be signed or unsigned, but signed real numbers are not legal in all contexts.

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A value consists of a real_number in parentheses, a *triple* in parentheses or an empty pair of parentheses. Empty parentheses indicate that no value is supplied for a particular data item. This is used primarily where a construct has a list of data items and it is desired to supply a value for an item further down the list but not for earlier items. The empty parentheses mark the places of the earlier items. An annotator shall take no action when it encounters empty parentheses. In particular, it shall not interpret this in the same way as a value of zero.

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A *triple* consists of one, two or three colon-separated real_numbers. Each real_number corresponds to a data value in one of three data sets, commonly used (in order) as values under best case/minimum, nominal/typical and worst case/maximum operating conditions. If a real_number is omitted, then a value is not included for that data set. At least one real_number is required. Both colons must always be present.

Apart from allowing negative numbers (signed_real_number instead of real_number), *rvalue* and *rtriple* are essentially the same as *value* and *triple*.

For specifying delay values, *delval* extends *rvalue* by allowing two or three *rvalue* constructs to be grouped in a further set of parentheses. When this is used, the first *rvalue* specifies the delay, as if a single *rvalue* were given. The second specifies the pulse rejection limit, or “r-limit,” associated with this delay. The third specifies the X-limit, or “e-limit.” This allows pulse control data to be associated in a uniform way with all types of delays in SDF, i.e., **IOPATH**, **PORT**, **INTERCONNECT**, **NETDELAY**, and **DEVICE** delays. Note that since any *rvalue* can be an empty pair of parentheses, each type of delay data can be annotated or omitted as the need arises.

The meaning of *delval* constructs in an *delval_list* is different for lists of length one, two, three, six, or twelve. Lists of length four or five are interpreted in the same way as lists of length six with trailing empty parentheses. Similarly, lists of length seven to eleven are interpreted in the same way as lists of length twelve with trailing empty parentheses. A complete discussion of the use of *delval_list* is included in 5.4.1.

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3.2.10 Operators

Operators are single-, double-, or triple-character sequences and are used in expressions.

The equality operators used in SDF conditional port expressions and timing check conditions return a logical value representing the result of the comparison, which is 1 for TRUE and 0 for FALSE, but can also be X.

`a == b` (logical equality) will be TRUE (1) only if a and b are of known logical state (0 or 1) and equal and FALSE (0) only if a and b are known and not equal. If either a or b is X or Z, then the result shall be X.

`a != b` (logical inequality) will be TRUE (1) only if a and b are known and not equal and FALSE (0) only if a and b are known and equal. If either a or b is X or Z, then the result will be X.

`a === b` (case equality) will be TRUE (1) if a and b are of the exact same logical state, including the X and Z states, and FALSE (0) otherwise.

`a !== b` (case inequality) will be TRUE (1) if a and b are of different logical states, including the X and Z states, and FALSE (0) otherwise.

4. SDF in the design process

4.1 Sharing of timing data

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By accessing an SDF file, Electronic Design Automation (EDA) tools are assured of consistent, accurate, and up-to-date data. This means that EDA tools can use data created by other tools as input to their own processes. Sharing data in this way, layout tools can use design constraints identified during timing analysis, and simulation tools can use the post-layout delay data.

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The EDA tools create, read from (to update their design), and write to SDF files.

4.2 Using multiple SDF files in one design

SDF files support hierarchical timing annotation. A design hierarchy might include several different ASICs (and/or cells or blocks within ASICs), each with its own SDF file (see Figure 1).

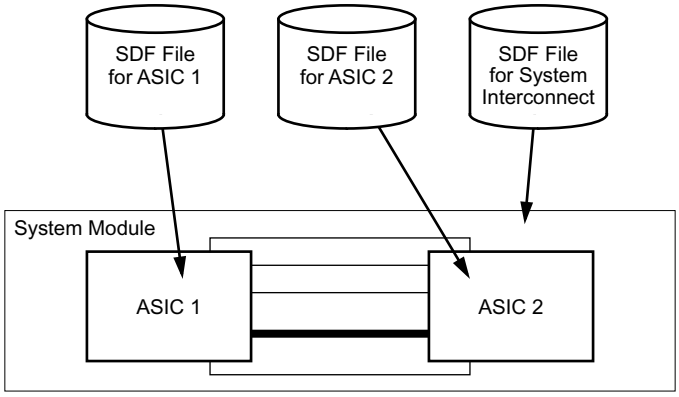

Figure 1—Multiple SDF files in a hierarchical design

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4.3 Timing data and constraints

SDF contains constructs for the description of computed timing data for back-annotation and the specification of timing constraints for forward-annotation. There is no restriction on using both sets of constructs in the same file. Indeed, some design synthesis tools (such as floorplanners) may need access to computed timing data as well as the timing constraints intended to be meet.

Subclauses 4.5 and 4.6 discuss the use of SDF for backward- and forward-annotation of timing information.

4.4 Timing environments

SDF includes constructs for describing the intended timing environment in which a design operates. For example, a waveform to be applied at clock inputs and the arrival time of primary inputs can be specified using SDF.

4.5 Back-annotation of timing data for design analysis

Figure 2 shows the use of SDF in back-annotating timing data to an analysis tool. An advantage of this approach is that once an SDF file has been created for a design, all analysis and verification tools can access the same timing data, which ensures consistency. Note, however, that different tools can have different restrictions in the way in which the data in an SDF file is used. For example, static timing analysis tools may be able to take into account path delays that have a negative value, whereas dynamic timing simulation tools may have to interpret such negative delays as zero. Even though by using SDF the timing data used by each tool is the same, differences in tool capabilities can nevertheless result in small differences in analysis results.

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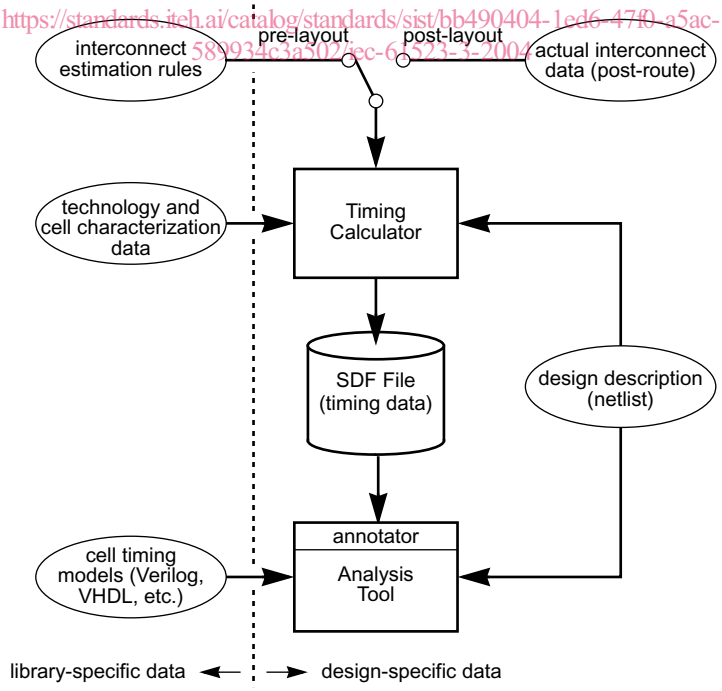

Figure 2—SDF files in timing back-annotation

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