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Behavioural languages –

Part 5:
VITAL ASIC (application specific integrated circuit) modeling specification

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FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
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International Standard IEC/IEEE 61691-5 has been processed through IEC technical committee 93: Design automation.

The text of this standard is based on the following documents:

IEEE Std	FDIS	Report on voting
1076.4 (2000)	93/194/FDIS	93/199/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives.

The committee has decided that the contents of this publication will remain unchanged until 2005.

IEC 61691 consists of the following parts, under the general title *Behavioural languages:*

IEC/IEEE 61691-1-1, Part 1: *VHDL language reference manual*

IEC 61691-2, Part 2: *VHDL multilogic system for model interoperability*

IEC 61691-3-1, Part 3-1: *Analog description in VHDL* (under consideration)

IEC 61691-3-2, Part 3-2: *Mathematical operation in VHDL*

IEC 61691-3-3, Part 3-3: *Synthesis in VHDL*

IEC 61691-3-4, Part 3-4: *Timing expressions in VHDL* (under consideration)

IEC 61691-3-5, Part 3-5: *Library utilities in VHDL* (under consideration)

IEC/IEEE 61691-4, Part 4: *Verilog® hardware description language*

IEC/IEEE 61691-5, Part 5: *VITAL ASIC (application specific integrated circuit) modeling specification*

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This Dual Logo International Standard is the result of an agreement between the IEC and the Institute of Electrical and Electronics Engineers, Inc. (IEEE). The original IEEE Standard was submitted to the IEC for consideration under the agreement, and the resulting IEC/IEEE Dual Logo International Standard has been published in accordance with the ISO/IEC Directives.

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IEEE Standard for VITAL ASIC (Application Specific Integrated Circuit) Modeling Specification

Sponsor

Design Automation Standards Committee
of the
IEEE Computer Society

Approved 21 September 2000

IEEE-SA Standards Board

Abstract: The VITAL (VHDL Initiative Towards ASIC Libraries) ASIC Modeling Specification is defined in this standard. This modeling specification defines a methodology which promotes the development of highly accurate, efficient simulation models for ASIC (Application-Specific Integrated Circuit) components in VHDL.
Keywords: ASIC, computer, computer languages, constraints, delay calculation, HDL, modeling, SDF, timing, Verilog, VHDL

IEEE Introduction

The objectives of the VITAL (VHDL Initiative Towards ASIC Libraries) initiative can be summed up in one sentence:

Accelerate the development of sign-off quality ASIC macrocell simulation libraries written in VHDL by leveraging existing methodologies of model development.

The VITAL ASIC modeling specification is a revision of the IEEE 1076.4-1995, IEEE Standard for VITAL ASIC Modeling Specification. Several new modeling enhancements have been added to the standard and several usability issues which have been raised with the 1995 standard have been addressed. The new enhancements and usability improvements addressed include:

— Standardized ASIC memory models
— Support of IEEE VHDL93 and SDF 1497 standards
— Multisource interconnect timing simulation
— SKEW constraint timing checks
— Timing constraint checks feature enhancements
— Additional generics to control 'X' generation and message reporting for glitches and timing constraints.
— Negative constraint calculation enhancement for vector signals to support memory models
— Fast delay path disable
— Negative glitch preemption

These new features will improve the functional, timing accuracy significantly and aid performance of gate level VHDL simulations.

The major enhancement is the definition of a ASIC memory modeling standard. With the addition of memory model package VITAL_Memory, a standard is defined which allow memory models to be coded in VHDL more efficiently. The standard VITAL memory model package provides a method to represent memories, procedures and functions to perform various operations and the definition of a modeling style that promotes consistency, maintainability and tool optimization. This standard does not define modeling behavior of specific memories. The scope of the memory model standard is currently restricted to ASIC memory modeling requirement for static RAMs and ROMs. The VITAL memory modeling enhancements are specified in Clause 10 through Clause 12. The VITAL standard memory package is found in Clause 13.

The memory model standard is derived from contributed work from the LSI Logic VHDL behavioral model and Mentor Graphics Memory Table Model (MTM) techniques. The generous support of VHDL International provided the needed funding to take these two contributed works and convert them into the memory specification and package code by the IEEE 1076.4 TAG (Technical Action Group) with significant contribution coming from leading EDA services company GDA Technologies.

The technical direction of the working group as well as the day to day activities of issue analysis and drafting of proposed wordings for the specification are the responsibility of the IEEE 1076.4 TAG. This group consists of Ekambaram Balaji, Prakash Bare, Nitin Chowdhary, Jose De Castro, Martin Gregory, Rama Kowsalya, B. Sudheendra Phani Kumar, William Yam, David Lin, Ashwini Mulgaonkar, Ajayharsh P. Varikat, and Steve Wadsworth and is chaired by Dennis B. Brophy. Without the dedication and hard work of this group it would not have been possible to complete this work.

The VITAL effort germinated from ideas generated at the VHDL International Users' Forum held in Scottsdale, Arizona in May 1992. Further discussions brought people to the conclusion that the biggest impediment to VHDL design was the lack of ASIC libraries; and that the biggest impediment to ASIC library

development was the lack of a uniform, efficient method for handling timing in VHDL. Since this problem had already been solved for other languages it was clear that a solution in VHDL was possible and that an effective way to arrive at this solution was to leverage existing technology. Leveraging existing tools and environments is viewed as a catalyst for the rapid deployment of ASIC libraries once this initiative is standardized under the IEEE.

The 1076.4 Working Group has a large membership of over three hundred interested people who have made significant contributions to this work through their participation in technical meetings, their review of technical data both in print and through electronic media, and their votes which guided and finally approved the content of the draft specification. This group is chaired by Victor Berman.

The VITAL ASIC modeling specification is the result of numerous discussions with ASIC vendors, EDA tool vendors, and ASIC designers to determine the requirements for effective design and fabrication of ASICS using VHDL. The highest priority issues identified by this group were:

— Timing accuracy
— Model maintainability
— Simulation performance

Some basic guiding principles followed during the entire specification development process were:

— To describe all functionality and timing semantics of the model entirely within the VHDL model and the associated VITAL packages except for multi-source interconnect.
— To provide a set of modeling rules (Level 1) which constrain the use of VHDL to a point that is amenable for simulator optimizations, and at the same time provide enough flexibility to support most existing modeling scenarios.
— To have all timing calculations (load dependent or environmentally dependent) performed outside of the VITAL model. The VITAL model would get these timing values solely as actual values to the model's generic parameter list or via SDF direct import.

BEHAVIOURAL LANGUAGES –

Part 5: VITAL ASIC (application specific integrated circuit) modeling specification

1. Overview

This clause describes the purpose and organization of this standard.

1.1 Scope

To provide a standard method of modeling ASICs in VHDL. This method is aimed at providing efficient, accurate, and tool independent simulation suitable for large chip-level designs typical of those which are based on ASICs.

1.2 Purpose

Current industry methods for designing complex chip-level designs rely on proprietary solutions which are based on specific commercial tools. This standard provides an effective means of performing those designs in a standard, non-proprietary manner that is independent of specific tools. This promotes cost effective design flows and promotes healthy levels of competition in the electronic design industry. This standard builds on the work of IEEE 1076 VHDL which is a standard hardware description language designed to allow such tool independent electronic design.

1.3 Intent of this standard

The intent of this standard is to accurately define the Draft Standard VITAL ASIC Modeling Specification. The primary audiences of this standard are the implementors of tools supporting the specification and ASIC modelers.

1.4 Structure and terminology of this standard

This standard is organized into clauses, each of which focuses on some particular area of the definition of the specification. Each page of the formal definition contains ruler-style line numbers in the left margin. Within each clause, individual constructs or concepts are discussed in each subclause.

Each subclause describing a specific construct or concept begins with an introductory paragraph. If applicable, the syntax of the construct is then described using one or more grammatical productions. A set of paragraphs describing in narrative form the information and rules related to the construct or concept then follows. Finally, each subclause may end with examples, figures, and notes.

1.5 Syntactic description

The form of a VITAL compliant VHDL description is described by means of a context-free syntax, using a simple variant of the Backus Naur Form (BNF); in particular:

a) Lower cased words, some containing embedded underlines, are used to denote syntactic categories, for example:

    VITAL_process_statement

    Whenever the name of a syntactic category is used, apart from the syntax rules themselves, spaces take the place of underlines (thus, "VITAL process statement" would appear in the narrative description when referring to the above syntactic category).

b) Boldface words are used to denote reserved words, for example:

    process

    Reserved words shall be used only in those places indicated by the syntax.

c) A *production* consists of a *left-hand side*, the symbol "::=" (which is read as "can be replaced by"), and a *right-hand side*. The left-hand side of a production is always a syntactic category; the right-hand side is a replacement rule.

    The meaning of a production is a textual-replacement rule: any occurrence of the left-hand side may be replaced by an instance of the right-hand side.

d) A vertical bar separates alternative items on the right-hand side of a production unless it occurs immediately after an opening brace, in which case it stands for itself.

e) Square brackets enclose optional items on the right-hand side of a production.

f) Braces enclose a repeated item or items on the right-hand side of a production. The items may appear zero or more times; the repetitions occur from left to right as with an equivalent left-recursive rule.

g) If the name of any syntactic category starts with an italicized part, it is equivalent to the category name without the italicized part. The italicized part is intended to convey some semantic information. For example, *unrestricted_variable*_name is syntactically equivalent to name alone.

h) The term simple_name is used for any occurrence of an identifier that already denotes some declared entity.

i) A syntactic category for which no replacement rule is specified is assumed to correspond to the VHDL syntactic category of the same name. In this case the appropriate replacement rule can be found in the IEEE Std 1076-1993 VHDL LRM.

j) A syntactic category beginning with the unitalicized prefix "VITAL_" represents a subset of a VHDL syntactic category.

1.6 Semantic description

The meaning of a particular construct or concept and any related restrictions are described with a set of narrative rules immediately following any syntactic productions in the subclause. In these rules, an italicized term indicates the definition of that term, and an identifier appearing in Helvetica font refers to a definition in one of the VHDL or VITAL standard packages or in a VHDL model description. An identifier beginning with the prefix "VITAL" corresponds to a definition in a VITAL standard package.

Use of the words "is" or "shall" in such a narrative indicates mandatory weight. A non-compliant practice may be described as *erroneous* or as an *error*. These terms are used in these semantic descriptions with the following meaning:

erroneous: the condition described represents a non-compliant modeling practice; however, implementations are not required to detect and report this condition. Conditions are deemed erroneous only when it is either very difficult or impossible in general to detect the condition during the processing of a model.

error: the condition described represents a non-compliant modeling practice; implementations are required to detect the condition and report an error to the user of the tool.

1.7 Front matter, examples, figures, notes, and annexes

Prior to this clause are several pieces of introductory material; following the final clause are some annexes and an index. The front matter, annexes, and index serve to orient and otherwise aid the user of this manual but are not part of the definition of the Draft Standard VITAL ASIC Modeling Specification.

Some subclauses of this definition contain examples, figures, and notes; with the exception of figures, these parts always appear at the end of a subclause. Examples are meant to illustrate the possible forms of the construct described. Figures are meant to illustrate the relationship between various constructs or concepts. Notes are meant to emphasize consequences of the rules described in the clause or elsewhere. In order to distinguish notes from the other narrative portions of the definition, notes are set as enumerated paragraphs in a font smaller than the rest of the text. Examples, figures, and notes are not part of the definition of the specification.

2. References

This clause lists the standards upon which this standard depends. Bibliographic references may be found in Annex C. Citations of the form "[C1]" refer to items listed in Annex C, not to items listed in this clause.

IEEE Std 1076-1993, IEEE Standard VHDL Language Reference Manual.[1]

NOTE An updated edition (2002) has been issued.

IEEE Std 1164-1993, IEEE Standard Multivalue Logic System for VHDL Model Interoperability (Std_logic_1164).

IEEE P1497, Draft Standard Delay Format Specification.

[1]IEEE publications are available from the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331, USA (http://standards.ieee.org/).