

# INTERNATIONAL STANDARD

# NORME INTERNATIONALE

Plasma display panels –  
Part 3-2: Interface – Electrical interface

STANDARD PREVIEW  
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Panneaux d'affichage à plasma –  
Partie 3-2: Interface – Interface électrique

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## PLASMA DISPLAY PANELS –

Part 3-2: Interface –  
Electrical interface

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| 110/181/FDIS | 110/190/RVD      |

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## PLASMA DISPLAY PANELS –

### Part 3-2: Interface – Electrical interface

#### 1 Scope

This part of IEC 61988 defines the electrical interface of digital video data signals, synchronization signals and functional signals between the image processing board of the PDP set and the control board of the PDP module, and defines the description of the pin assignment of the connectors.

#### 2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61988-1, *Plasma display panels – Part 1: Terminology and letter symbols*

IEC 61988-2-1, *Plasma display panels – Part 2-1: Measuring methods – Optical*

IEC 61988-2-2, *Plasma display panels – Part 2-2: Measuring methods – Optoelectrical*

TIA/EIA-644A, *Electrical characteristics of low voltage differential signaling (LVDS) interface circuits*

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JEIDA-59-1999, *Digital interface standards for monitor* (only available in English)

#### 3 Terms, definitions and abbreviations

##### 3.1 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 61988-1, IEC 60068-1 and IEC 60107-1 as well as the following apply.

##### 3.1.1

##### **image processing board**

circuit board including A/D converter, scaler and video decoder, deinterlacing for image signal from input device such as TV-tuner, PC, DVD, etc.

##### 3.2 Abbreviations

NOTE The following are acronyms for reference.

|      |  |
|------|--|
| TTL  | Transistor-transistor logic                  |
| LVDS | Low voltage differential signalling          |
| TMDS | Transition minimized differential signalling |
| HS   | Horizontal synchronization                   |
| VS   | Vertical synchronization                     |
| DE   | Data enable                                  |
| DCLK | Data clock                                   |
| APC  | Auto power control                           |

## 4 Electrical interface requirements

The electrical interface of PDP module is a power sequence and a digital interface of PDP module.

The power sequence of PDP module is power on- and off-sequence of all power supplies in and to PDP module. The power on- and off-sequence of PDP module shall be fully described in each relevant specification.

The digital signal interface is either an LVDS, a TTL or a TMDS interface, whose signal encodes the digital video data and function control signals.

Function control signal, which is the additional signal, except digital video signal, to control the functions such as APC, shall be fully described in each detail specification.

The interface configuration, input signal definition, pin assignment, input signal timing and power requirement shall be described in each detail specification.

## 5 Electrical interface of digital signal

### 5.1 Basic configuration

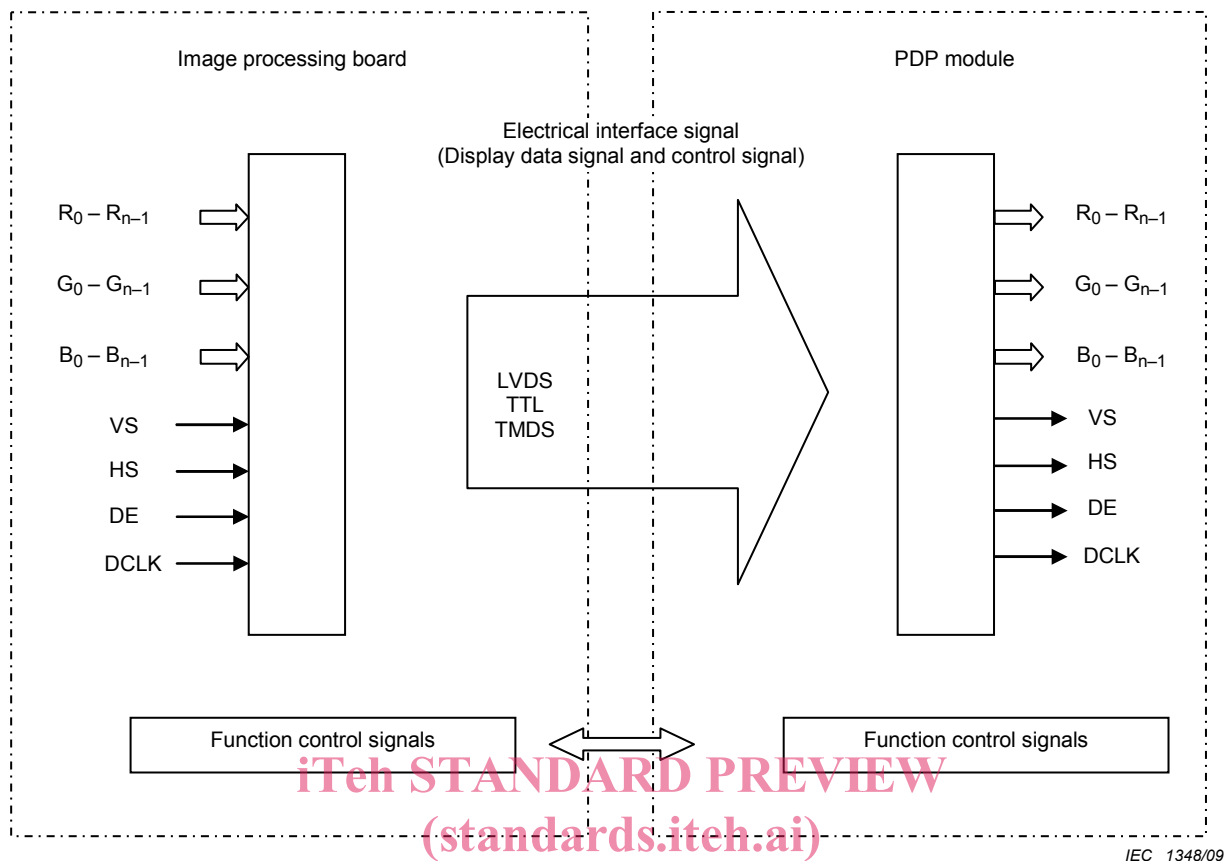
The basic configuration of electrical interface of digital signal is shown in Figure 1 as one of examples. Examples of LVDS, TTL and TMDS are explained in Annex A.

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NOTE 1 The image processing board includes A/D converter, scaler and video decoder for image signal from input device such as TV-tuner, PC, DVD, etc.

NOTE 2  $R_i$ ,  $G_i$  and  $B_i$ :  $i$ th bit data for  $n$ -bit digital video signal of red, green and blue, respectively ( $i=0$  to  $n-1$ ).

**Figure 1 – Block diagram of an example interface of data signal**

## 5.2 Interface input signal definition

The example of interface signal definition and function is as follows in Table 1.

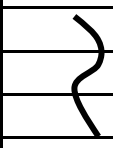

**Table 1 – Example of interface signal function**

| Symbol   | I/O | Function   | Description                 |
|--|-----|--|-----------------------------|
| Rx IN0+<br>(or RA+)  | I   | Display data signal:<br>R <sub>0</sub> , R <sub>1</sub> , R <sub>2</sub> , R <sub>3</sub> , R <sub>4</sub> , R <sub>5</sub> , G <sub>0</sub>         | LVDS differential data (+)  |
| Rx IN0 -<br>(or RA-)   | I   |  | LVDS differential data (-)  |
| Rx IN1+<br>(or RB+)  | I   | Display data signal:<br>G <sub>1</sub> , G <sub>2</sub> , G <sub>3</sub> , G <sub>4</sub> , G <sub>5</sub> , B <sub>0</sub> , B <sub>1</sub>         | LVDS differential data (+)  |
| Rx IN1 -<br>(or RB-)   | I   |  | LVDS differential data (-)  |
| Rx IN2+<br>(or RC+)  | I   | Display data signal:<br>B <sub>2</sub> , B <sub>3</sub> , B <sub>4</sub> , B <sub>5</sub> , HS,<br>VS, DE  | LVDS differential data (+)  |
| Rx IN2 -<br>(or RC-)   | I   |  | LVDS differential data (-)  |
| Rx IN3+<br>(or RD+)  | I   | Display data signal and control signal:<br>R <sub>6</sub> , R <sub>7</sub> , G <sub>6</sub> , G <sub>7</sub> , B <sub>6</sub> , B <sub>7</sub> , RES | LVDS differential data (+)  |
| Rx IN3 -<br>(or RD-)   | I   |  | LVDS differential data (-)  |
| Rx IN4+<br>(or RE+)  | I   | Display data signal and control signal:<br>B <sub>8</sub> , B <sub>9</sub> , G <sub>8</sub> , G <sub>9</sub> , R <sub>8</sub> , R <sub>9</sub> , RES | LVDS differential data (+)  |
| Rx IN4-<br>(or RE-)  | I   |  | LVDS differential data (-)  |
| Rx CLKIN+<br>(or CLK+)   | I   | Data clock signal:<br>DCLK   | LVDS differential clock (+) |
| Rx CLKIN-<br>(or CLK-)   | I   |  | LVDS differential clock (-) |
| NOTE This example shows the case of LVDS with 10-bit video signal. |     |  |                             |

### 5.3 Pin assignment

The pin assignments should be given in the form of Table 2.

**Table 2 – Example of connector pin assignments**

| Pin no  | Pin name  |
|---|---|
| 1   | GND   |
| 2   | GND   |
| 3   | Rx IN0-   |
| 4   | Rx IN0+   |
| 5   | GND   |
| 6   | GND   |
| 7   | Rx IN1-   |
| 8   | Rx IN1+   |
| 9   | GND   |
| 10  | GND   |
| 11  | Rx IN2-   |
| 12  | Rx IN2+   |
| 13  | GND   |
| 14  | GND   |
| 15  | Rx CLKIN-   |
| 16  | Rx CLKIN+   |
| 17  | GND   |
| 18  | GND   |
| 19  | Rx IN3-   |
| 20  | Rx IN3+   |
| 21  | GND   |
| 22  | GND   |
| 23  | GND   |
| 24  | GND   |
| 25  | Rx IN4-   |
| 26  | Rx IN4+   |
| 27  | GND   |
| 28  | GND   |
| 29  | GND   |
| 30  | GND   |
| 31  | GND   |
|  |  |
|   |   |

#### **5.4 Input signal timing**

Timing of the interface signals of the PDP module shall be fully described. An example is given in A.1.

#### **5.5 Power requirement**

Power requirements, and power on sequence when needed, shall be fully described. An example is given in A.1.1.

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## Annex A (informative)

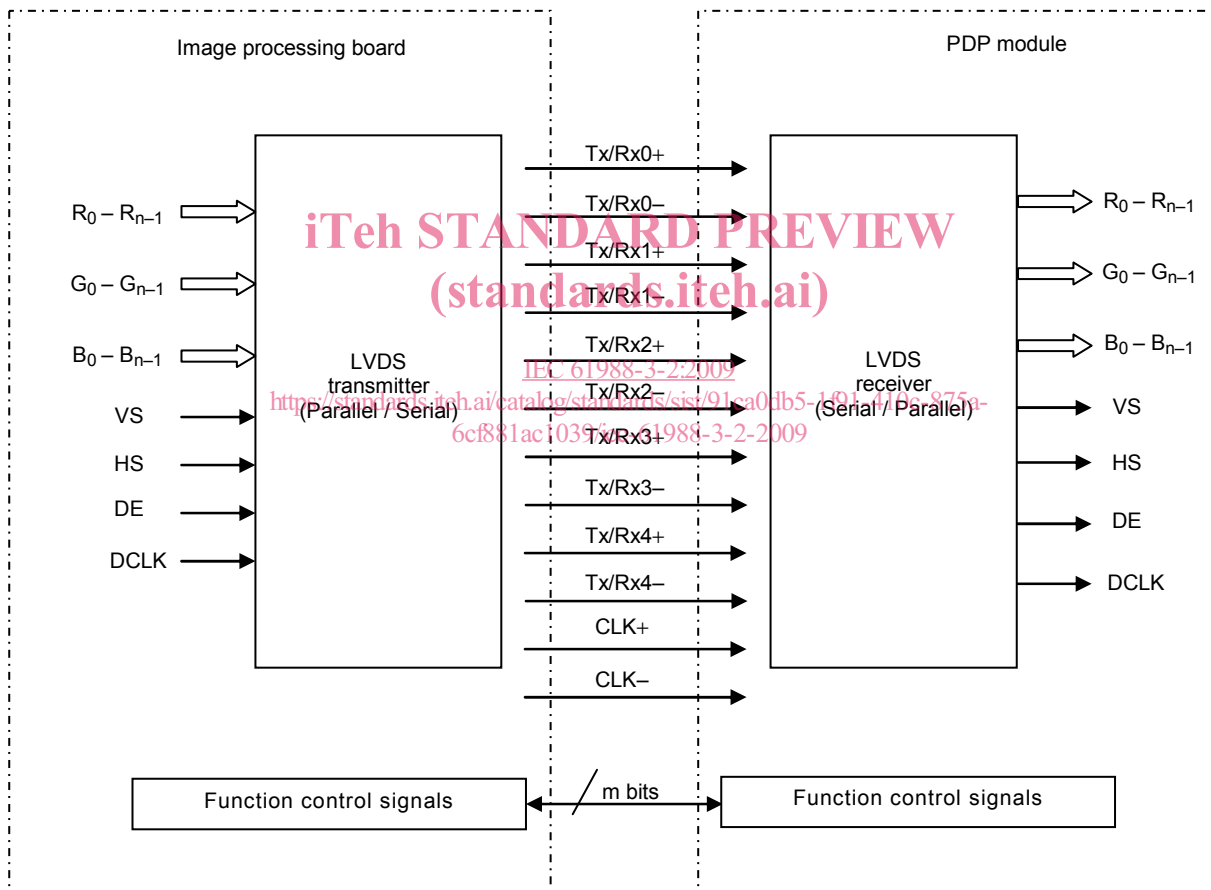
### LVDS, TTL and TMDS

#### A.1 Video

##### A.1.1 LVDS

##### A.1.1.1 Basic configuration

Figure A.1 shows an example of interface configuration of LVDS.



IEC 1349/09

Figure A.1 – Interface configuration

**A.1.1.2 Interface input signal specification**

The input signal (display data signal and control signal) is converted from parallel data to serial data with the LVDS transmitter and further converted into six sets of differential signals before input to the PDP module. The LVDS signal definition and function is as follows in Table A.1.

**Table A.1 – Signal definition and function**

| Symbol               | I/O | Function   | Description                 |
|----------------------|-----|--|-----------------------------|
| Rx IN0+ (or RA+)     | I   | Display data signal:<br>R <sub>0</sub> , R <sub>1</sub> , R <sub>2</sub> , R <sub>3</sub> , R <sub>4</sub> , R <sub>5</sub> , G <sub>0</sub>         | LVDS differential data (+)  |
| Rx IN0- (or RA-)     | I   |  | LVDS differential data (-)  |
| Rx IN1+ (or RB+)     | I   | Display data signal:<br>G <sub>1</sub> , G <sub>2</sub> , G <sub>3</sub> , G <sub>4</sub> , G <sub>5</sub> , B <sub>0</sub> , B <sub>1</sub>         | LVDS differential data (+)  |
| Rx IN1- (or RB-)     | I   |  | LVDS differential data (-)  |
| Rx IN2+ (or RC+)     | I   | Display data signal:<br>B <sub>2</sub> , B <sub>3</sub> , B <sub>4</sub> , B <sub>5</sub> , HS, VS, DE   | LVDS differential data (+)  |
| Rx IN2- (or RC-)     | I   |  | LVDS differential data (-)  |
| Rx IN3+ (or RD+)     | I   | Display data signal and control signal:<br>R <sub>6</sub> , R <sub>7</sub> , G <sub>6</sub> , G <sub>7</sub> , B <sub>6</sub> , B <sub>7</sub> , RES | LVDS differential data (+)  |
| Rx IN3- (or RD-)     | I   |  | LVDS differential data (-)  |
| Rx IN4+ (or RE+)     | I   | Display data signal and control signal:<br>B <sub>8</sub> , B <sub>9</sub> , G <sub>8</sub> , G <sub>9</sub> , R <sub>8</sub> , R <sub>9</sub> , RES | LVDS differential data (+)  |
| Rx IN4- (or RE-)     | I   |  | LVDS differential data (-)  |
| Rx CLKIN+ (or DCLK+) | I   | Data clock signal: DCLK  | LVDS differential clock (+) |
| Rx CLKIN- (or DCLK-) | I   |  | LVDS differential clock (-) |

**A.1.1.3 Pin assignment**

The pin names may be given in the form of Table A.2.

**Table A.2 – Connector pin assignment**

| Pin no | Pin name  |
|--------|-----------|
| 1      | GND       |
| 2      | GND       |
| 3      | Rx IN0-   |
| 4      | Rx IN0+   |
| 5      | GND       |
| 6      | GND       |
| 7      | Rx IN1-   |
| 8      | Rx IN1+   |
| 9      | GND       |
| 10     | GND       |
| 11     | Rx IN2-   |
| 12     | Rx IN2+   |
| 13     | GND       |
| 14     | GND       |
| 15     | Rx CLKIN- |
| 16     | Rx CLKIN+ |
| 17     | GND       |
| 18     | GND       |
| 19     | Rx IN3-   |
| 20     | Rx IN3+   |
| 21     | GND       |
| 22     | GND       |
| 23     | GND       |
| 24     | GND       |
| 25     | RX IN4-   |
| 26     | RX IN4+   |
| 27     | GND       |
| 28     | GND       |
| 29     | GND       |
| 30     | GND       |
| 31     | GND       |
|        |           |
|        |           |
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