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JEDEC STANDARD

Board Level Drop Test Method of Components for Handheld Electronic Products

JESD22-B111

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

JEDEC

EIA
Electronic Industries Alliance

INTERNATIONAL ELECTROTECHNICAL COMMISSION

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BOARD LEVEL DROP TEST METHOD OF COMPONENTS FOR HANDHELD ELECTRONIC PRODUCTS

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The text of this PAS is based on the following document:	This PAS was approved for publication by the P-members of the committee concerned as indicated in the following document
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BOARD LEVEL DROP TEST METHOD OF COMPONENTS FOR HANDHELD ELECTRONIC PRODUCTS

Introduction

The handheld electronic products fit into the consumer and portable market segments. Included in the handheld electronic products are cameras, calculators, cell phones, pagers, palm size PCs, Personal Computer Memory Card International Association (PCMCIA) cards, smart cards, mobile phones, personal digital assistants (PDAs) and other electronic products that can be conveniently stored in a pocket and used while held in user's hand.

These handheld electronic products are more prone to being dropped during their useful service life because of their size and weight. This dropping event can not only cause mechanical failures in the housing of the device but also create electrical failures in the printed circuit board (PCB) assemblies mounted inside the housing due to transfer of energy through PCB supports. The electrical failures may result from various failure modes such as cracking of circuit board, trace cracking on the board, cracking of solder interconnections between the components and the board, and the component cracks. The primary driver of these failures is excessive flexing of circuit board due to input acceleration to the board created from dropping the handheld electronic product. This flexing of the board causes relative motion between the board and the components mounted on it, resulting in component, interconnects, or board failures. The failure is a strong function of the combination of the board design, construction, material, thickness, and surface finish; interconnect material and standoff height; and component size.

BOARD LEVEL DROP TEST METHOD OF COMPONENTS FOR HANDHELD ELECTRONIC PRODUCTS

(From JEDEC Board Ballot JCB-03-38, formulated under the cognizance of the JC-14.1 Subcommittee on Reliability Test Methods for Packaged Devices)

1 Scope

The Board Level Drop Test Method is intended to evaluate and compare drop performance of surface mount electronic components for handheld electronic product applications in an accelerated test environment, where excessive flexure of a circuit board causes product failure. The purpose is to standardize the test board and test methodology to provide a reproducible assessment of the drop test performance of surface mounted components while duplicating the failure modes normally observed during product level test.

The purpose of this document is to prescribe a standardized test method and reporting procedure. This is not a component qualification test and is not meant to replace any system level drop test that maybe needed to qualify a specific handheld electronic product. The standard is not meant to cover the drop test required to simulate shipping and handling related shock of electronic components or PCB assemblies. These requirements are already addressed in JESD22-B104-B and JESD22-B110. The method is applicable to both area-array and perimeter-leaded surface mounted packages.

Correlation between test and field conditions is not yet fully established. Consequently, the test procedure is presently more appropriate for relative component performance than for use as a pass/fail criterion. Rather, results should be used to augment existing data or establish baseline for potential investigative efforts in package/board technologies.

The comparability between different test sites, data acquisition methods, and board manufacturers has not been fully demonstrated by existing data. As a result, if the data are to be used for direct comparison of component performance, matching study must first be performed to prove that the data are in fact comparable across different test sites and test conditions.

This method is not intended to substitute for full characterization testing, which might incorporate substantially larger sample sizes and increased number of drops. Due to limited sample size and number of drops specified here, it is possible that enough failure data may not be generated in every case to perform full statistical analysis.

2 Apparatus

As per JESD22-B104-B and JESDD22-B110

3 Terms and definitions

For purposes of this standard, the following definitions shall apply

component: A packaged semiconductor device.

single-sided PCB assembly: A printed circuit board assembly with components mounted on only one side of the board

double-sided PCB assembly: A printed circuit board assembly with components mounted on top and bottom sides of the board.

handheld electronic product: A product that can conveniently be stored in a pocket (of sufficient size) and used when held in user's hand.

NOTE Included in handheld electronic products are cameras, calculators, cell phones, pagers, palm-size PCs (formerly called 'pocket organizers'), Personal Computer Memory Card International Association (PCMCIA) cards, smart cards, mobile phones, personal digital assistants (PDAs), and other communication devices.

peak acceleration: The maximum acceleration during the dynamic motion of the test apparatus.

pulse duration; acceleration interval: The time interval between the instant when the acceleration first reaches 10% of its specified peak level and the instant when the acceleration first returns to 10% of the specified peak level after having reach that peak level.

table drop height: The free-fall drop height of the drop table needed to attain the prescribed peak acceleration and pulse duration.

event: An electrical discontinuity of resistance greater than 1000 ohms lasting for 1 microsecond or longer.

event detector: A continuity test instrument capable of detecting electrical discontinuity of resistance greater than 1000 ohms lasting for 1 microsecond or longer.

4 Applicable documents

JESD22-B104-B, *Mechanical Shock*
JESD22-B110, *Subassembly Mechanical Shock*
IPC-SMT-782, *Surface Mount Design and Land Pattern Standard*
IPC-A-600, *Acceptability of Printed Boards*
J-STD-020, *Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices*
J-STD-033, *Standard for Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices*
IPC-9701, *Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments*

5 Test Components and Board

5.1 Components

This standard covers all area arrays and perimeter-leaded surface-mountable packaged semiconductor devices such as BGAs, LGAs, CSPs, TSOPs, and QFNs typically used in handheld electronic product. Since components with body sizes larger than 15 mm x 15 mm in size are not used in these applications, the maximum size of the component body covered in this standard is 15 mm x 15 mm. All components used for this testing must be daisy-chained. The daisy chain should either be done at the die level or by providing daisy chain links at the lead-frame or substrate level. In case of non-daisy chain die, a mechanical dummy die must be used inside the package to simulate the actual structure of the package. The die size and thickness should be similar to the functional die size to be used in application. The component materials, dimensions, and assembly processes shall be representative of typical production device.

5.2 Test board

Since the drop test performance is a function of the test board used for evaluation, this standard defines a preferred test board construction, dimensions, and material that is representative of those used in handheld electronic products. If another board construction/material better represents a specific application, the test board construction, dimensions and material should be documented. The test data generated using such a board shall be correlated at least once by generating the same data on same component using the preferred board defined in this document.

5.2.1 Preferred board construction, material, and design

The preferred test board shall use built-up multilayer technology incorporating microvias using 1+6+1 stack-up. This is required as typical PCB assemblies used in handheld electronic systems are constructed using high density, buildup technology. The test board shall have a nominal thickness of 1.0 mm. Table 1 provides the thickness, copper coverage, and the material for each layer. The dielectric materials shall meet the mechanical properties requirements as given in Table 2. The PCB shall have Organic Solderability Preservatives (OSP) as surface finish to avoid any copper oxidation before component mounting. The glass transition temperature, Tg, of each dielectric material as well as of the composite board shall be 125 ^{o}C or greater. The modulus and Tg of the dielectric materials shall be specified. The composite values (Modulus, and Tg) shall be measured on at least one representative test board at component mounting location. The boards shall be symmetric in construction about the mid-plane of the board, except for the minor differences in the top and bottom two layers.

Since a typical product board may have a combination of microvia in pad and no vias in pad for area array packages for routing purposes, it is required that such components (BGAs, CSPs, etc) be tested on board with both microvia and non-microvia PCB pads. This shall be accomplished by designing double sided boards with mirror component footprint on each side (top and bottom) of the board. The board Side A shall have microvias in pads (“via in pad”) on all component mounting pads while the board Side B shall have no microvias in pads (“no via in pads”). For board Side A, the microvias in pads shall be created with laser ablation with via diameter of 110 microns. The vias shall then be plated resulting in straight or near straight walls. The capture pad diameter shall be at least 220 microns. Although two sided boards are to be designed, the component shall only be mounted on one side at a time, resulting in two single sided assemblies (“Side A assembly” and “Side B assembly”), unless the component is anticipated for use in mirror-sided board assemblies. In that case, the components shall be mounted on each side of the board.

5.2 Test board (cont'd)

5.2.1 Preferred board construction, material, and design)cont'd)

As perimeter-leaded devices do not typically require microvia in pad, the test board for such devices (TSOP, QFP, etc) does not need to include microvias. The board shall still be designed as double-sided with footprint of similar sized components on each side.

Although daisy-chain nets will typically not require plated though holes (PTH) other than those required for manual probe pads and connectors, the test board shall contain PTH in the component region (1.2X the area covered by component) to approximate mechanical effect of vias on actual application boards. There shall be 20 plated through holes per square centimeter in the component region. The actual location and distribution of plated through holes will depend on component size and I/O. The through holes shall have the drill diameter of 300 microns and finished plated hole diameter of 250 microns. The PTH pad diameters shall be 550 microns for the outer layer and 600 microns for the inner layers.

It is recommended that the component mounting pads on the PCB be designed as per the specification in Table 3 for area array devices. The pad design for leaded and perimeter I/O devices shall be according to IPC-SM-782 guidelines. All component attachment pads shall be non-solder-mask-defined (NSMD) with solder mask clearance of 75 microns between the edge of the pad and the edge of solder mask. Smaller clearance can be used as long as it does not cause any solder mask encroachment on pads due to mis-registration. Solder mask registration tolerance shall not exceed 50 microns

Table 1 — Test board stack-up and material

Board Layer	Thickness (microns)	Copper Coverage (%)	Material
Solder Mask	20		LPI
Layer 1	35	Pads + traces	Copper
Dielectric 1-2	65		RCC*
Layer 2	35	40% including daisy chain links	Copper
Dielectric 2-3	130		FR4†
Layer 3	18	70%	Copper
Dielectric 3-4	130		FR4†
Layer 4	18	70%	Copper
Dielectric 4-5	130		FR4†
Layer 5	18	70%	Copper
Dielectric 5-6	130		FR4†
Layer 6	18	70%	Copper
Dielectric 6-7	130		FR4†
Layer7	35	40%	Copper
Dielectric 7-8	65		RCC*
Layer 8	35	Pads + Traces + daisy chain links	Copper
Solder Mask	20		LPI

* Suggested RCC Material: Polyclad PCL-CF-400 12/35/35
† Suggested FR4 Material: NELCO N-4000-6 or equivalent